

Compal Confidential

NAT02 M/B Schematics Document

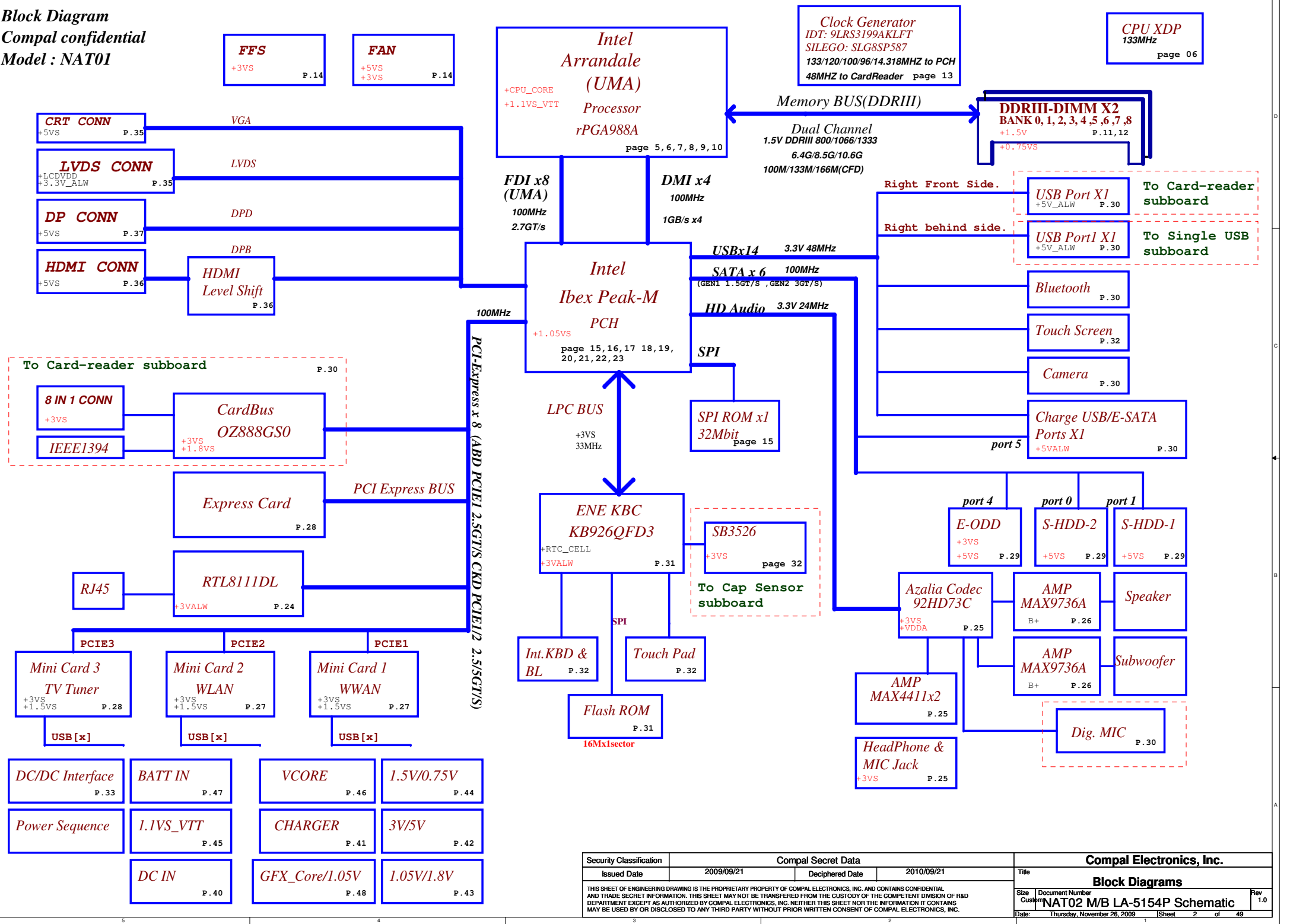
Intel Arrandale Processor with DDRIII + Ibex Peak-M

2009-11-26

REV : 1 . 0

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Block Diagram
Compal confidential
Model : NAT01



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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Graphic	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.1VS	1.1V power rail for PCIe of GUP	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
B+_BIAS	B+ always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

Device	Address	Device	Address
Smart Battery	0001 011X b	WWAN	
		WLAN	
		Express Card	

Device	Address
Clock Generator (9LRS3191AKLFT, SLG8SP585)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
Free Fall Sensor	
CPU XDP	
PCH XDP	remove
XDCP_ISL90727	0101 110Xb
XDCP_ISL90728	0111 110Xb

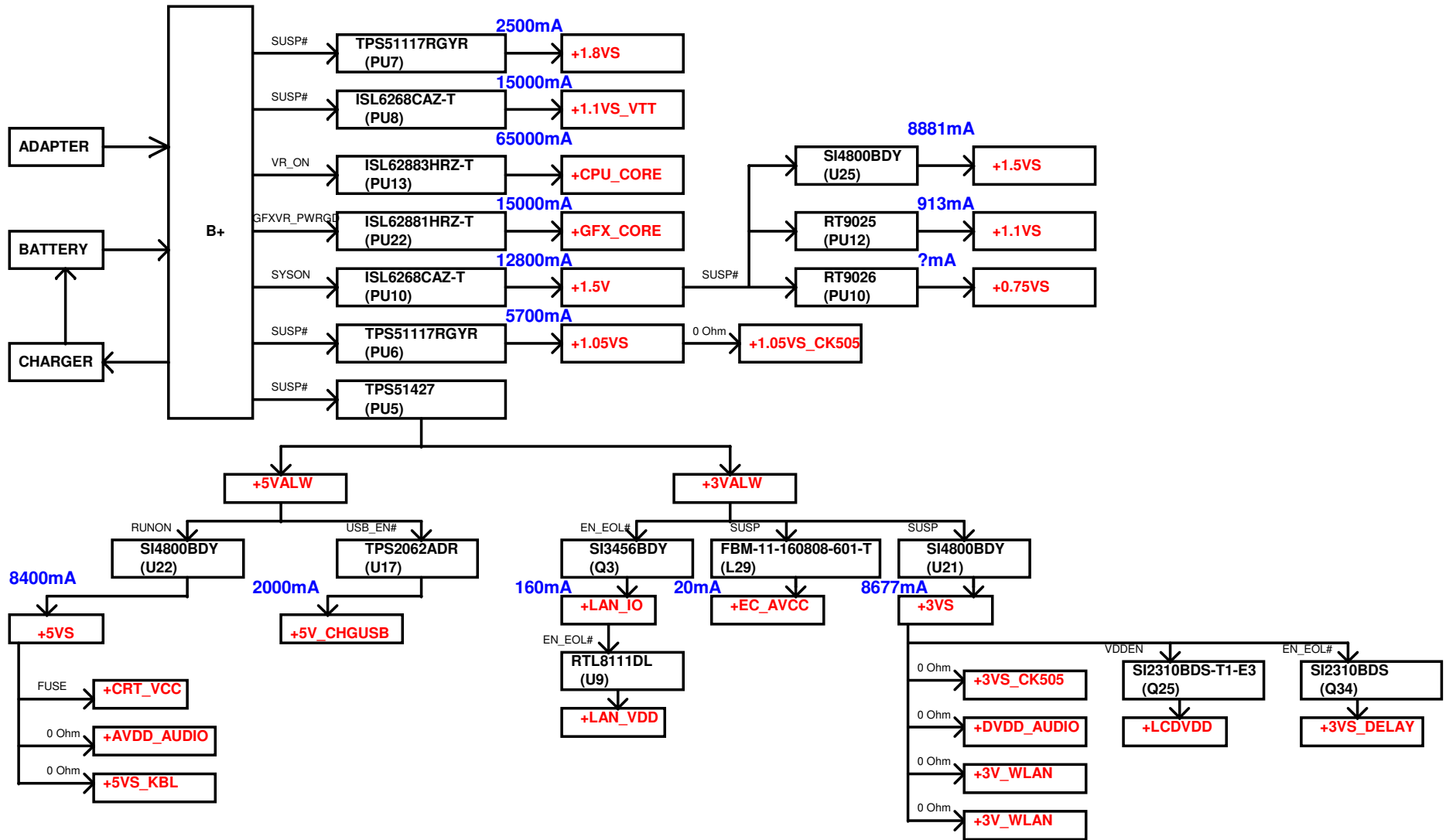
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

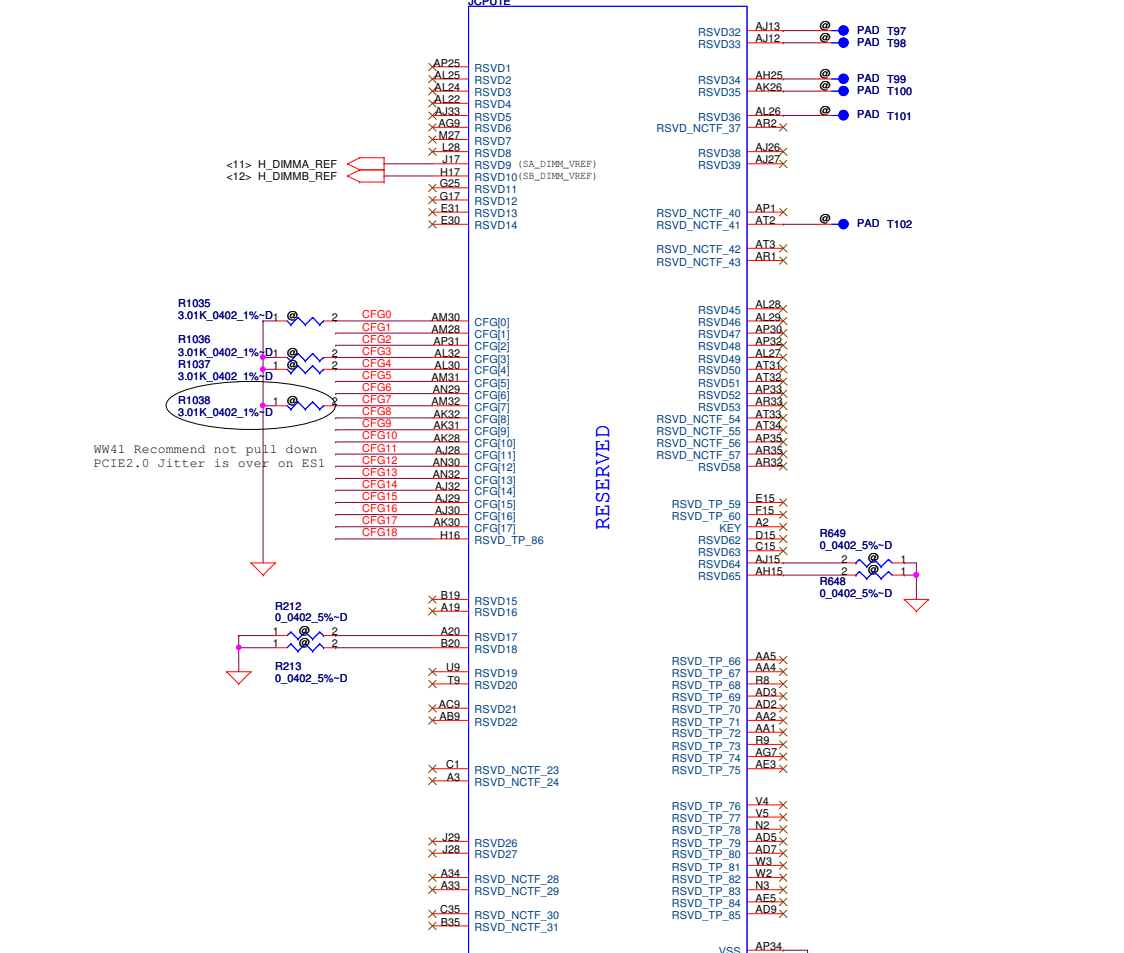
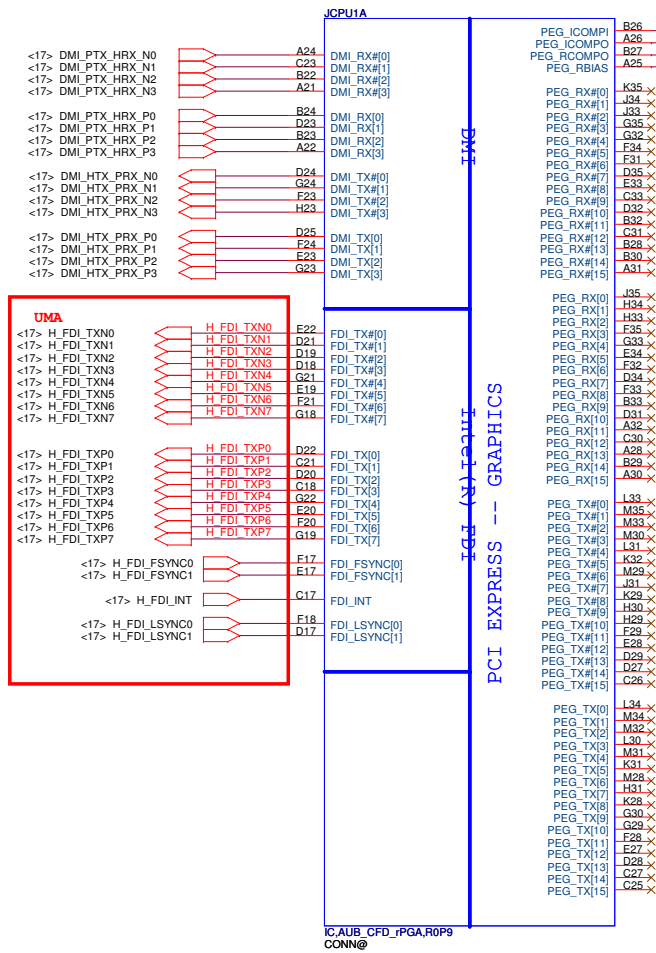
	Vcc	3.3V +/- 5%			
	Ra	100K +/- 1%			
Board ID	VGA	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
X00	M96	0	0 V	0 V	0.100 V
X01	M96	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
X02	M96	18K +/- 1%	0.436 V	0.503 V	0.538 V
MP	M96	33K +/- 1%	0.712 V	0.819 V	0.875 V
X00	Madison	56K +/- 1%	1.036 V	1.185 V	1.264 V
X01	Madison	100K +/- 1%	1.453 V	1.650 V	1.759 V
X02	Madison	200K +/- 1%	1.935 V	2.200 V	2.341 V
MP	Madison	NC	2.500 V	3.300 V	3.300 V

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

[illegible]

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CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

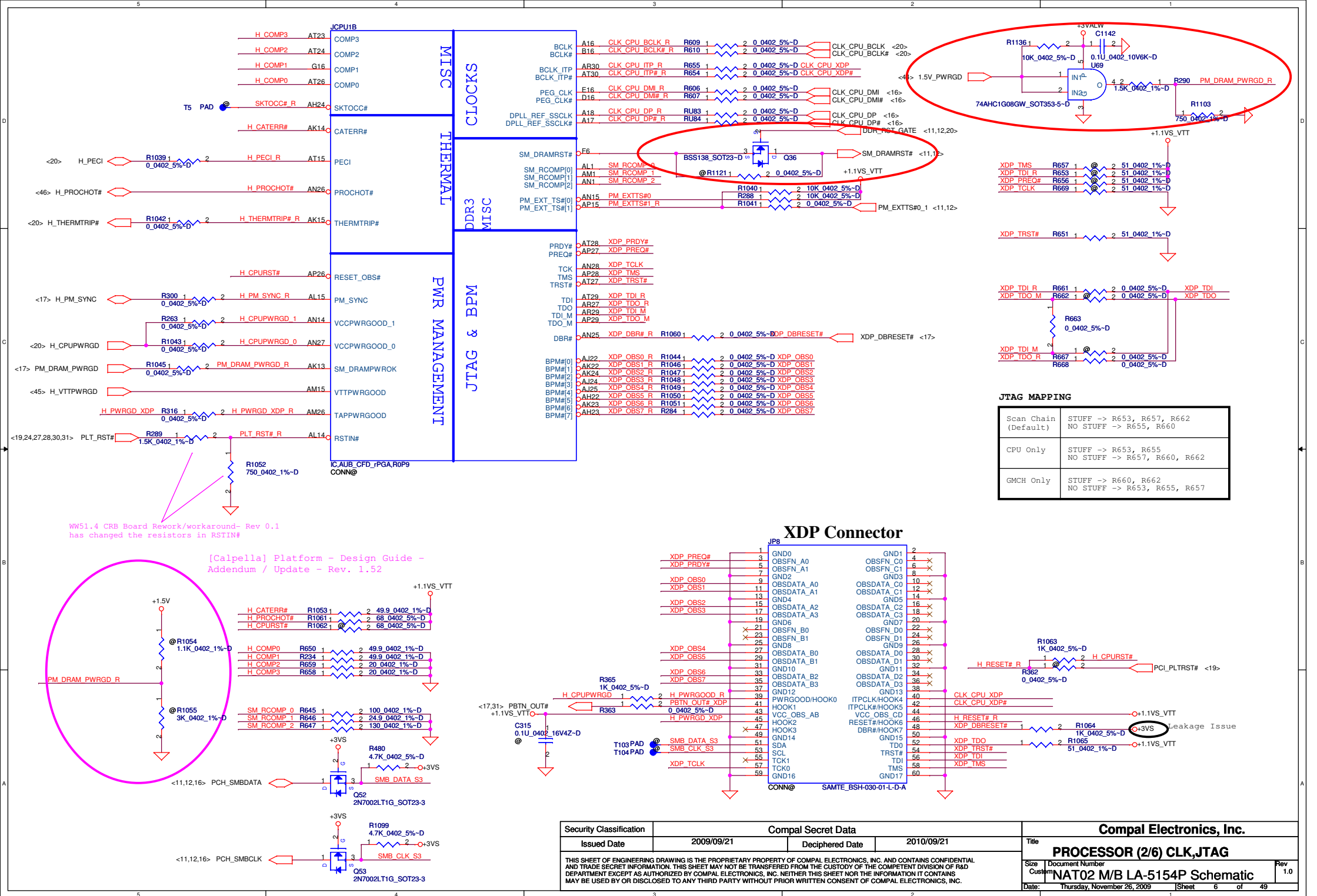
CFG3 - PCI-Express Static Lane Reversal

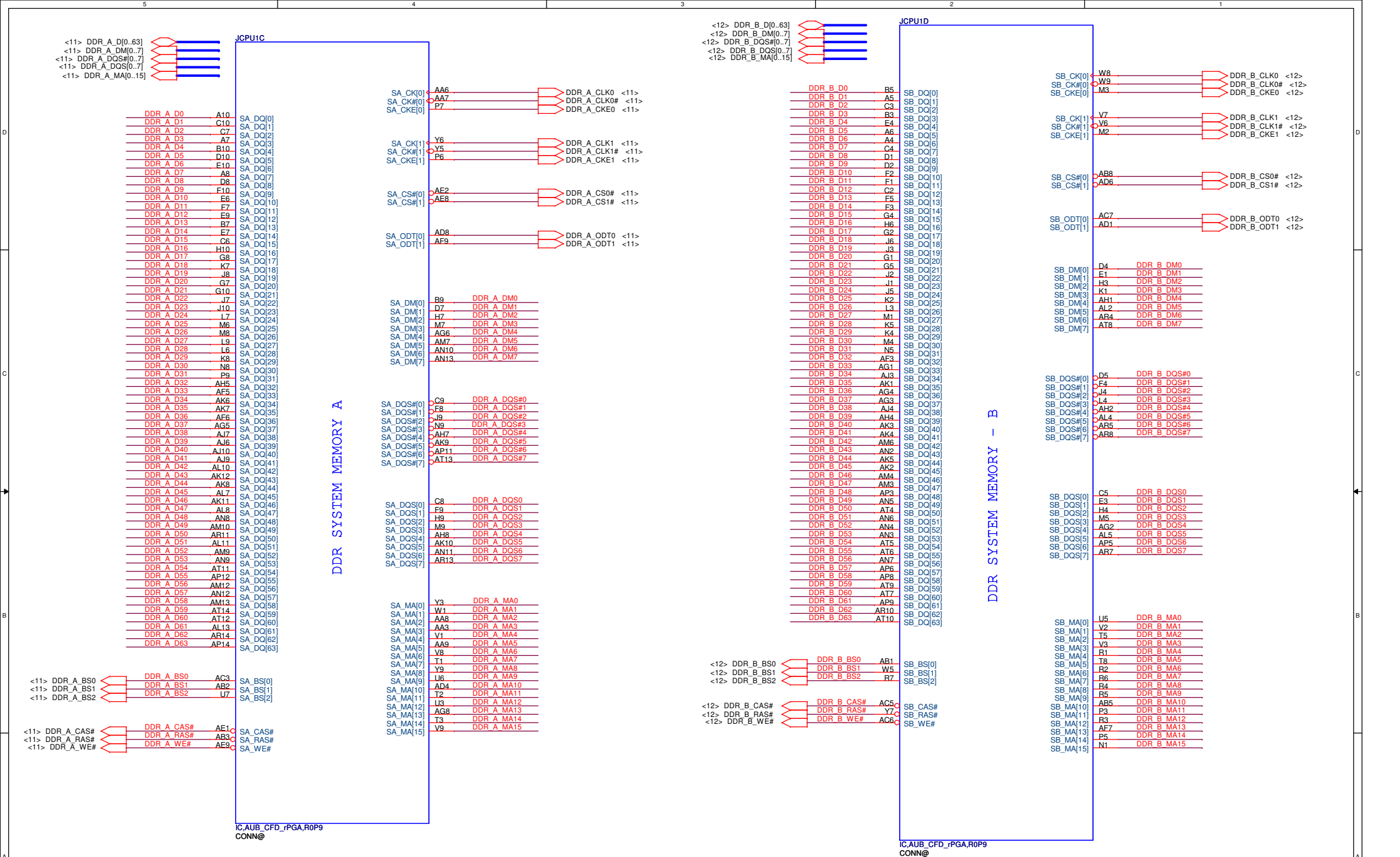
*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

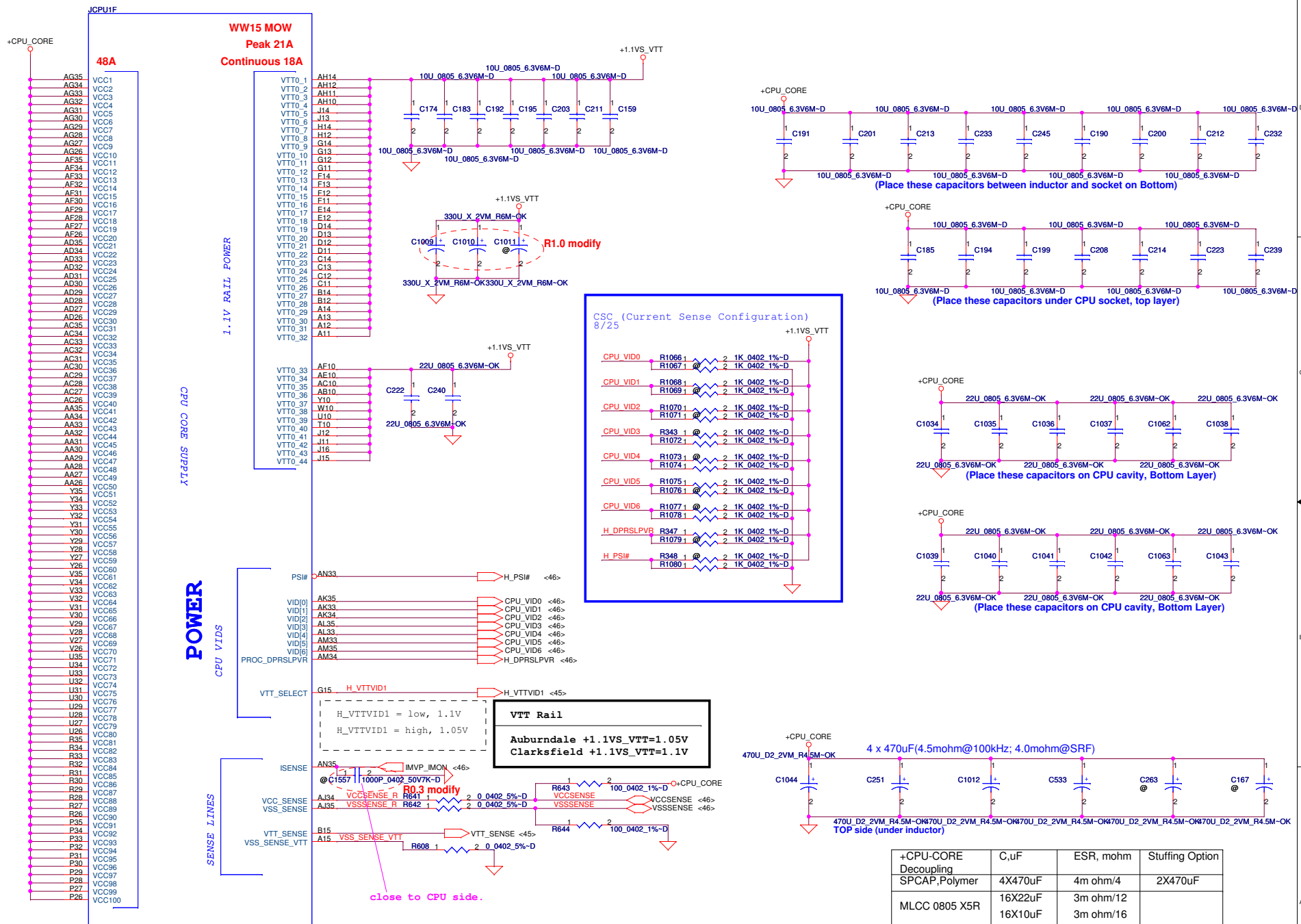
CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

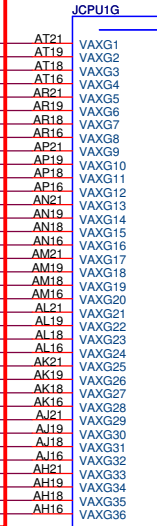
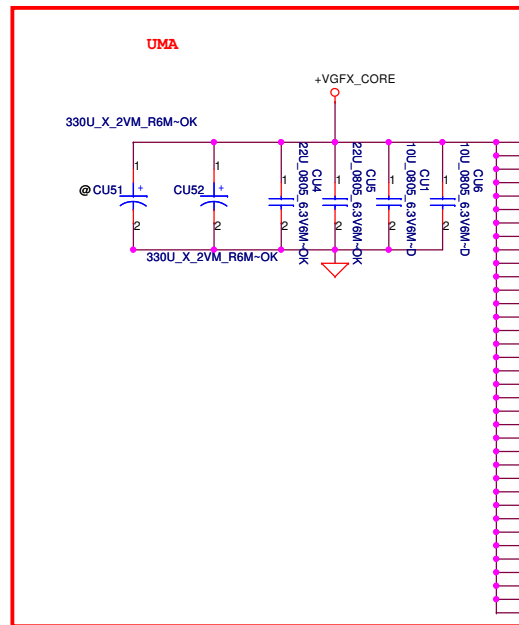






IC_AUB_CFD_PGA_R0P9
CONN@

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15A
GRAPHICS

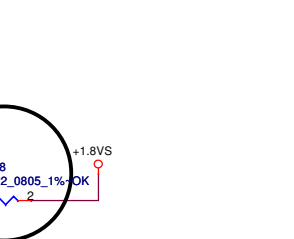
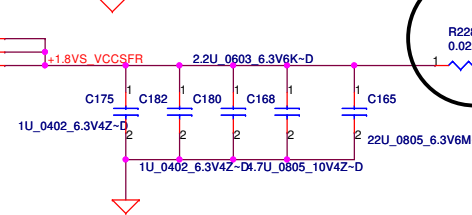
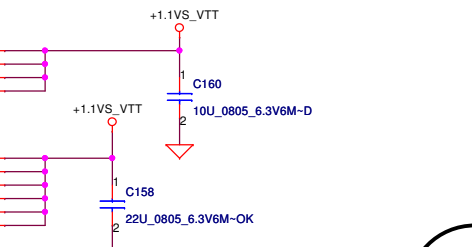
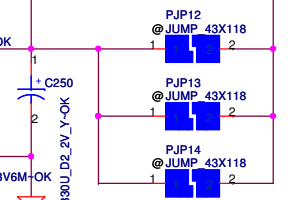
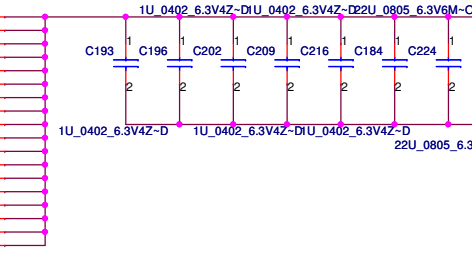
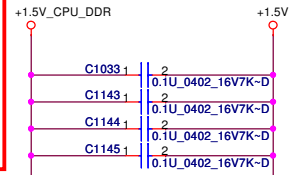
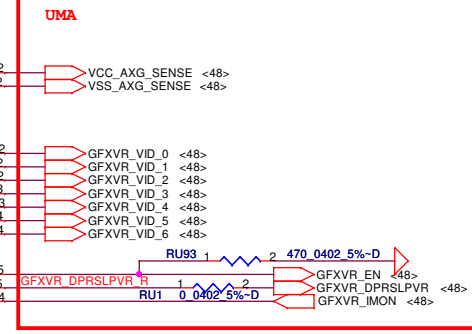
POWER

FDI

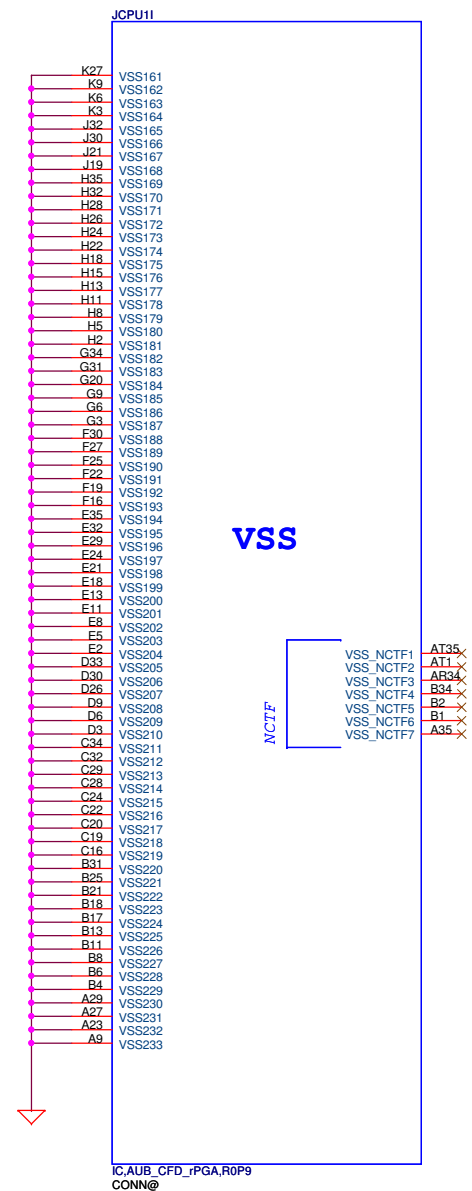
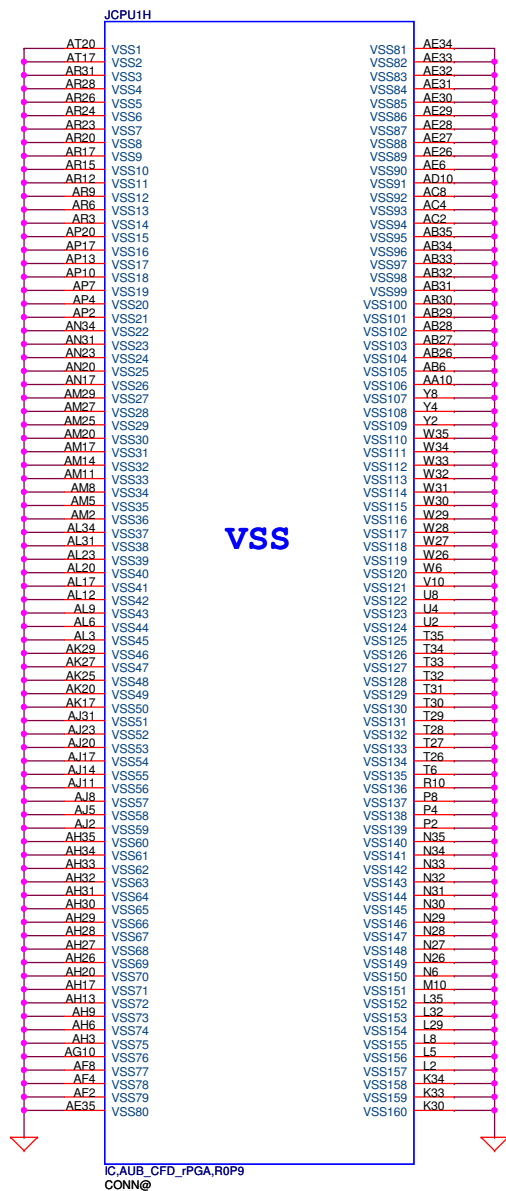
PEG & DMI

IC:AUB_CFD_rPGA,R0P9
CONN@

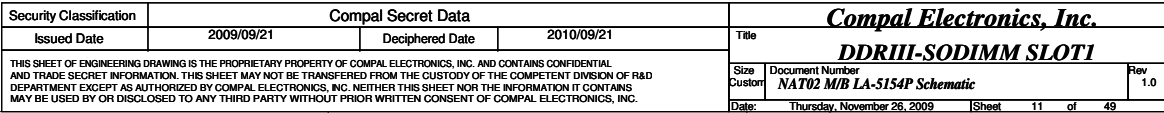
11/17 follow Intel suggest to change RU93 to 470 ohm

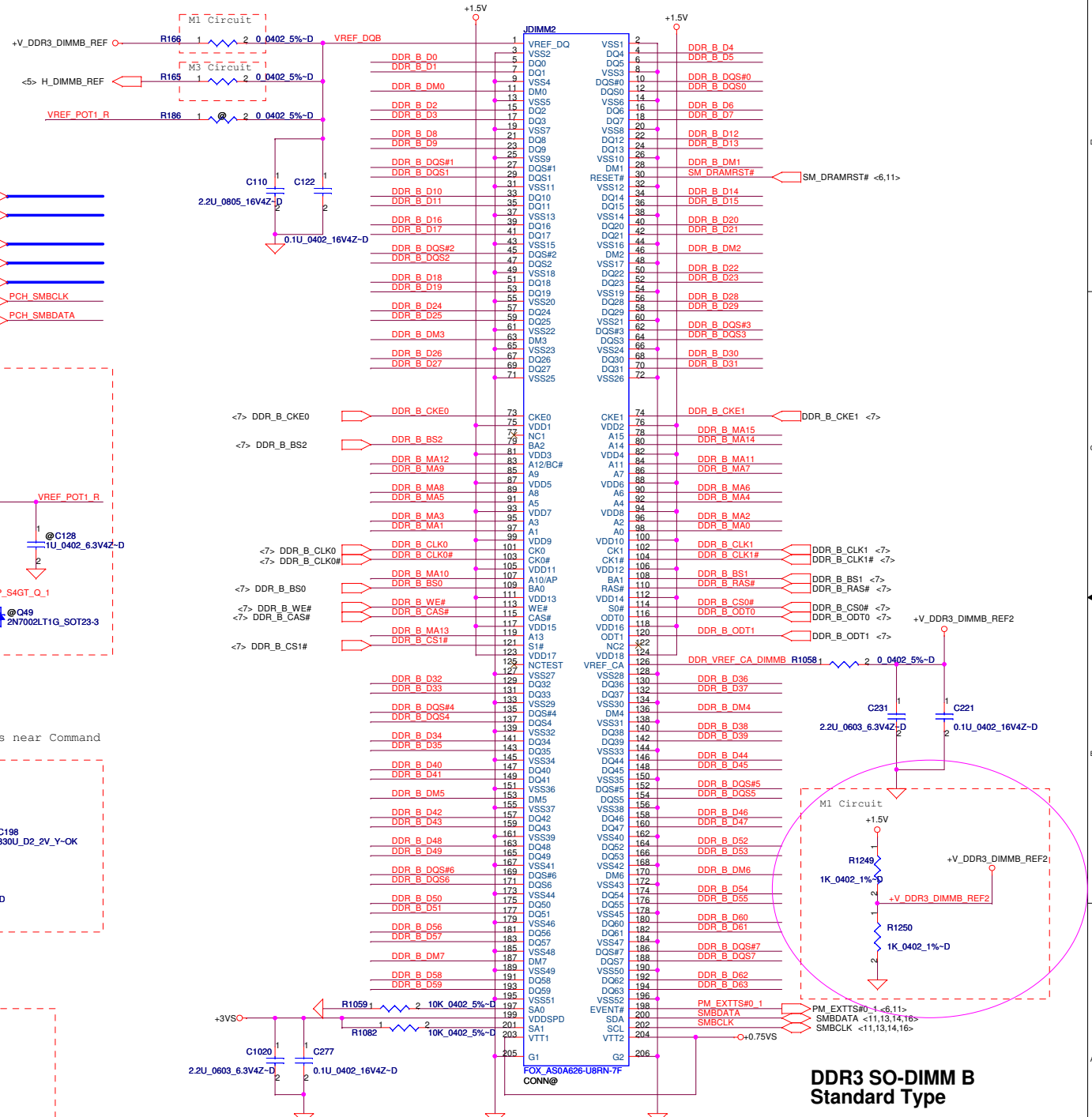


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Layout Note:
Place near JD

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

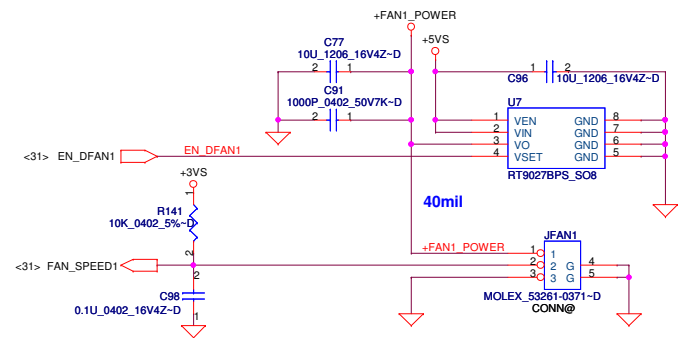
Layout Note:
Place near JDIMM2.203 & JDIMM2.204

DDR3 SO-DIMM B Standard Type

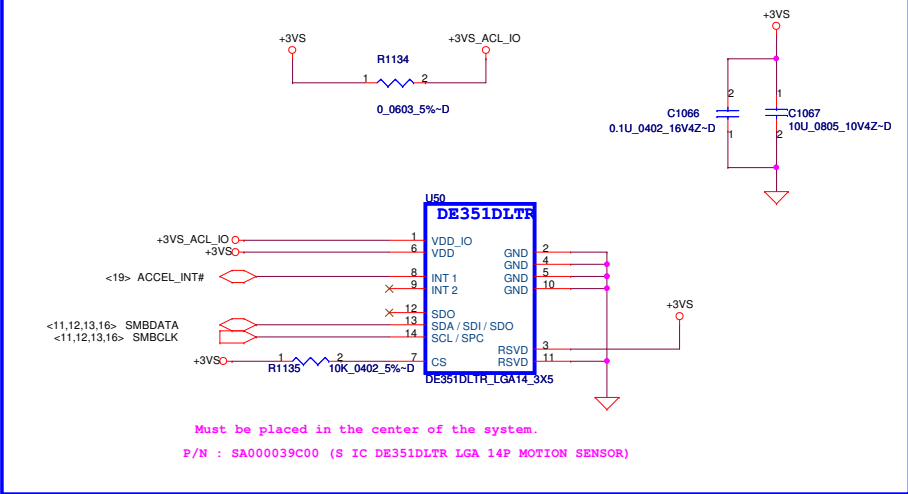
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DDRIII-SODIMM SLOT2

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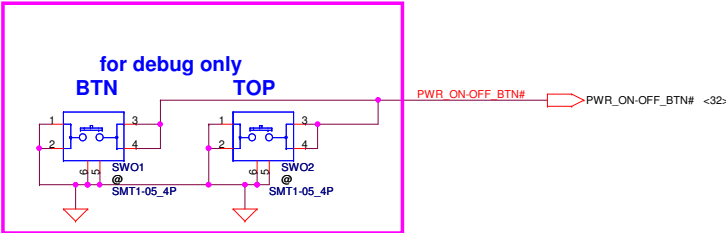
FAN Control circuit



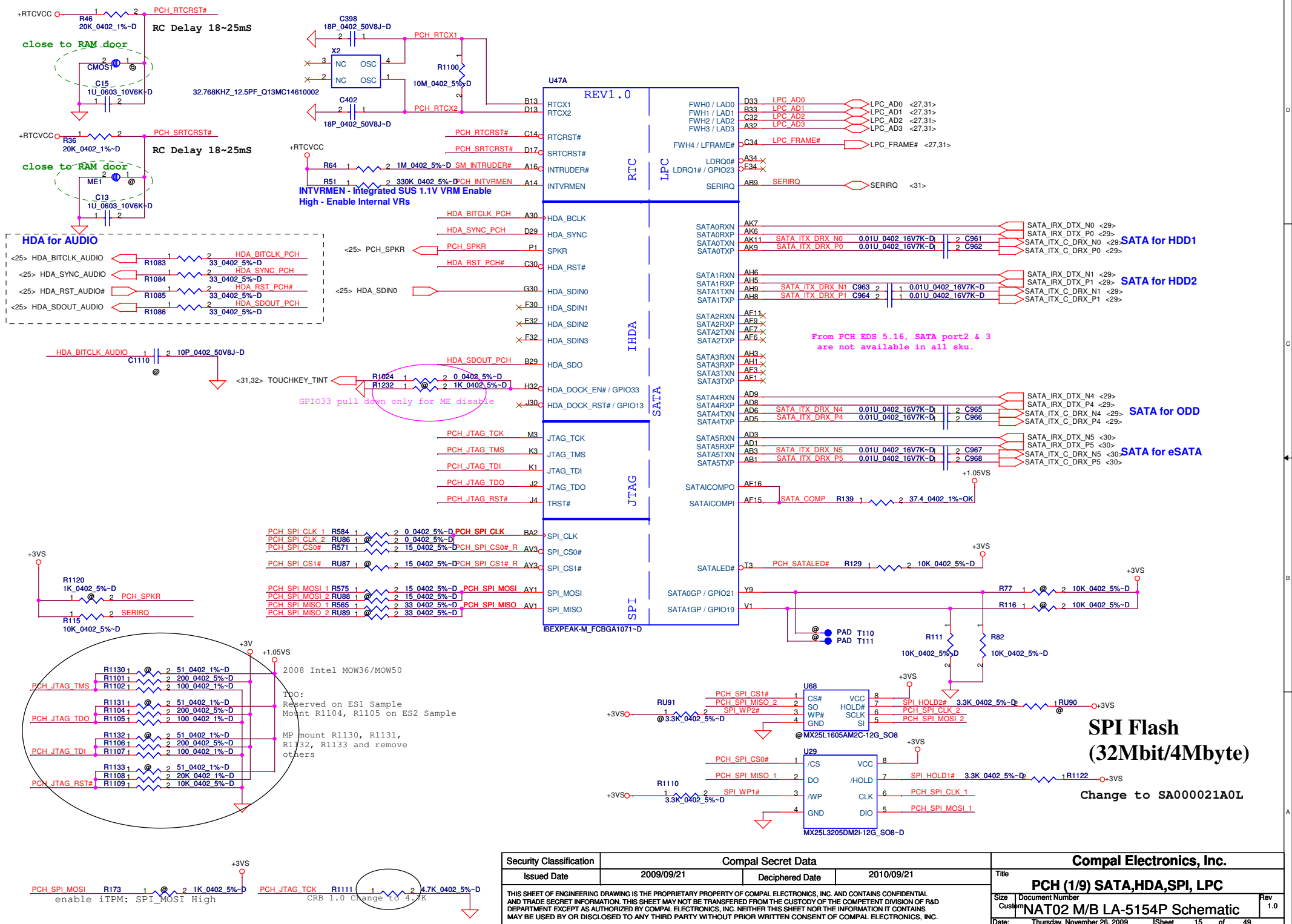
Free Fall Sensor



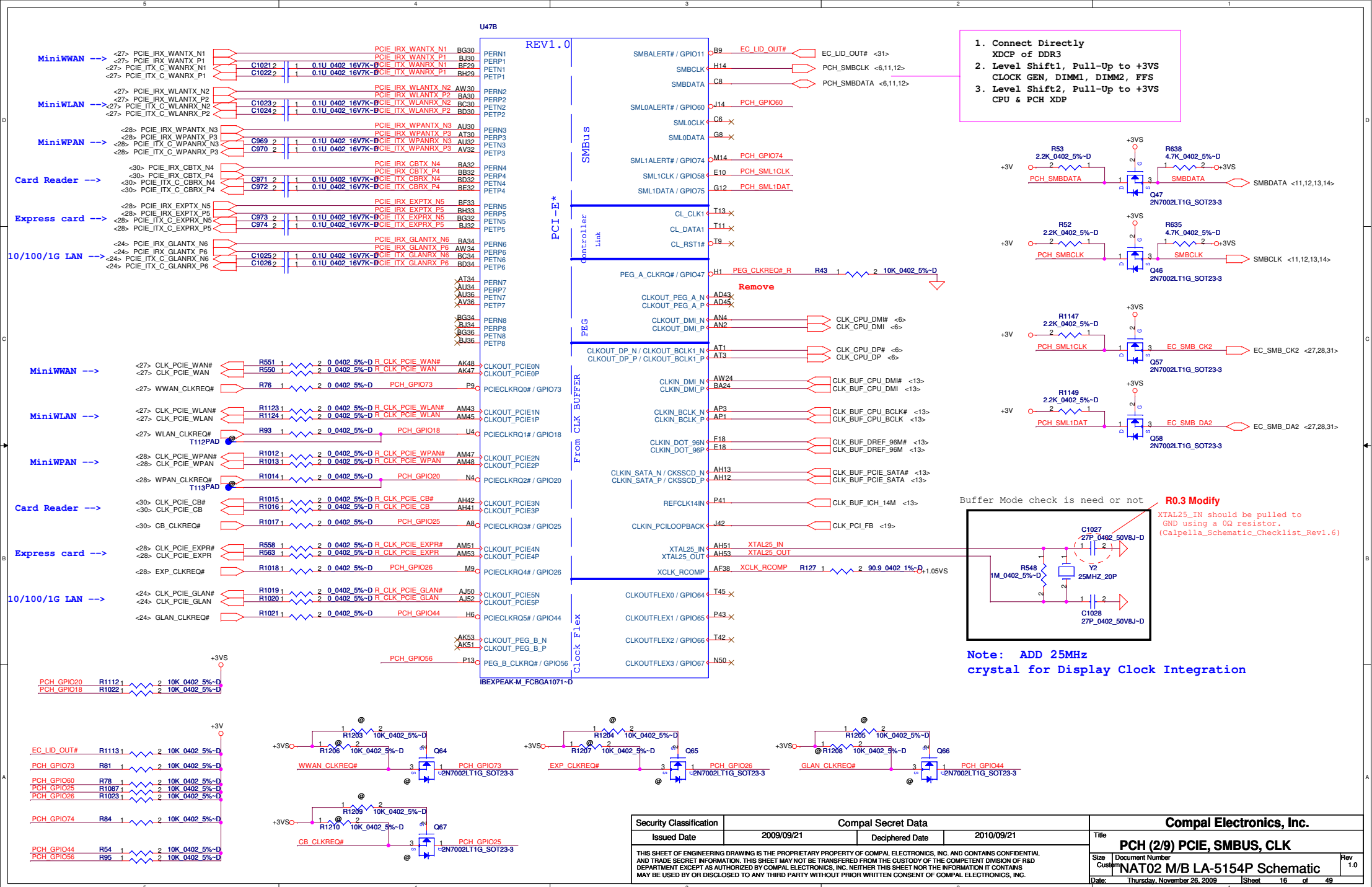
Power Button



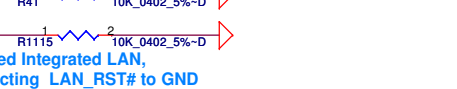
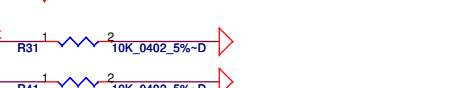
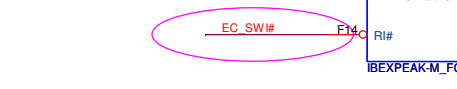
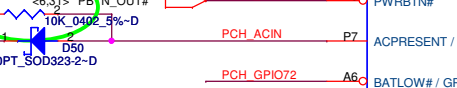
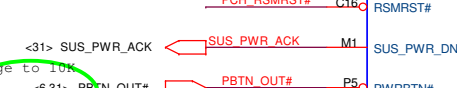
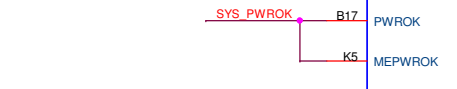
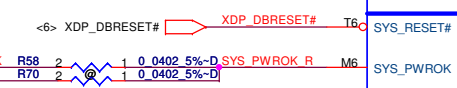
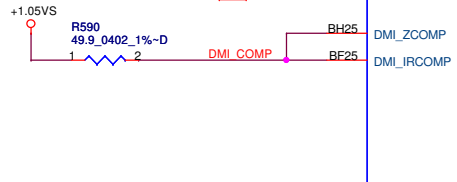
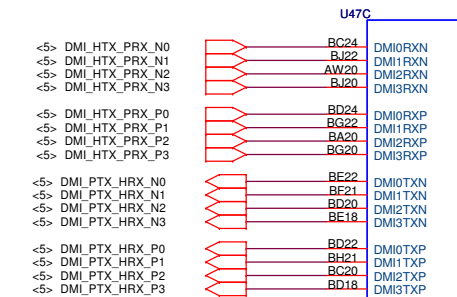
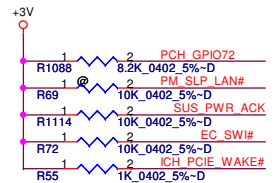
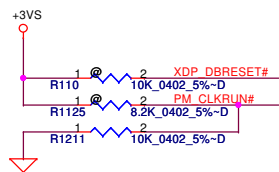
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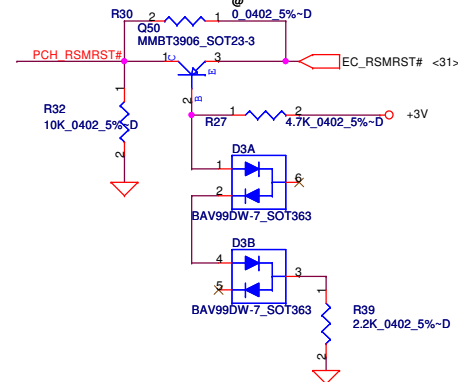
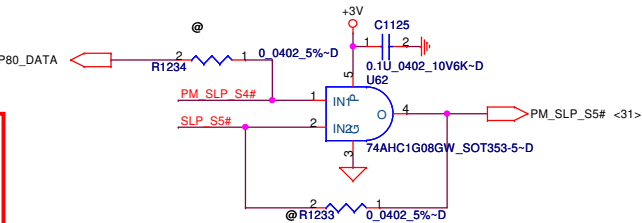
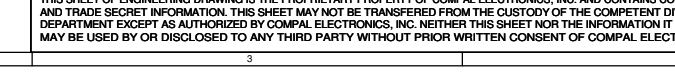
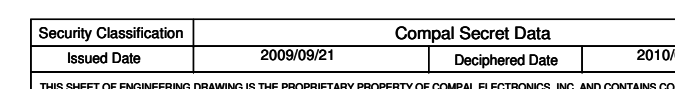
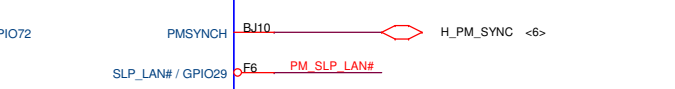
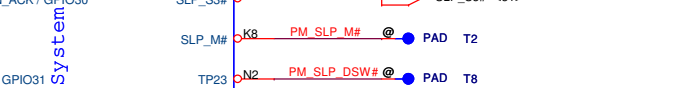
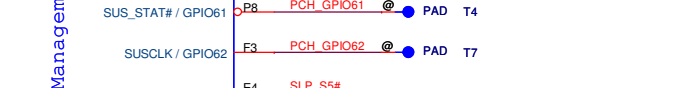
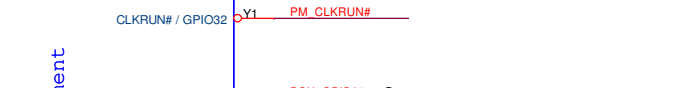
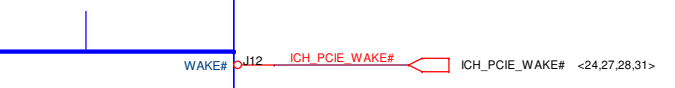
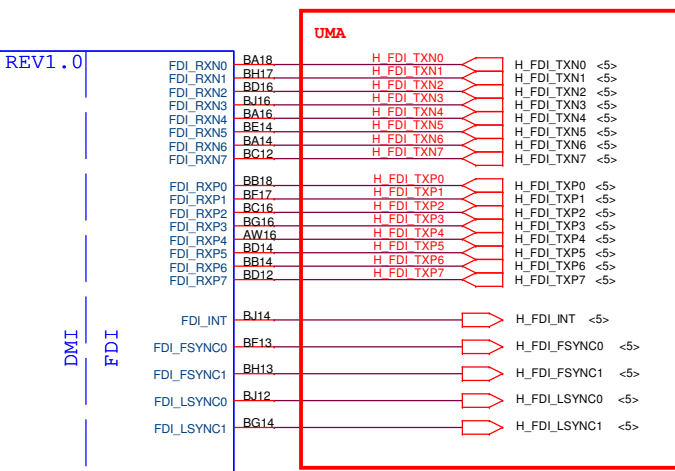
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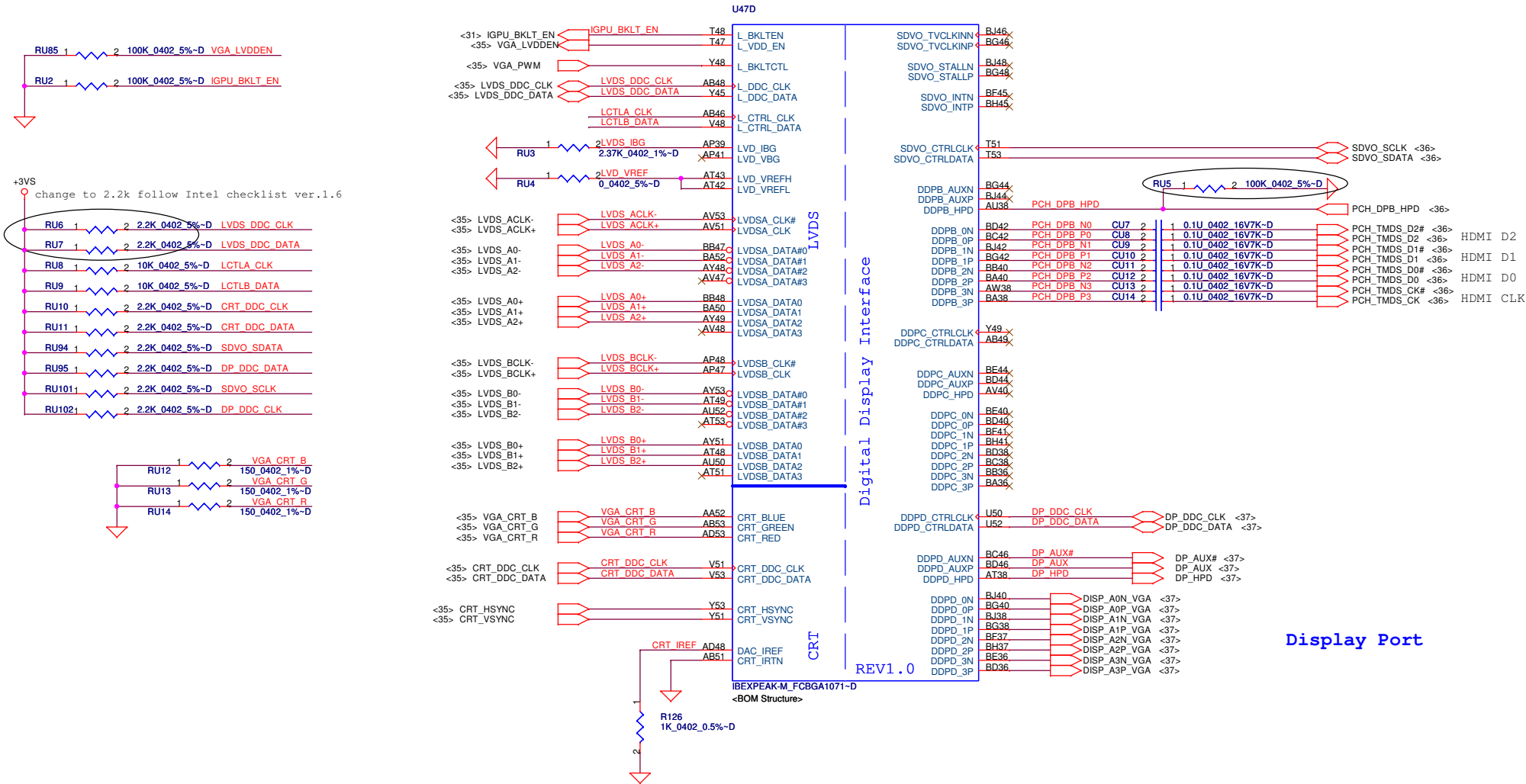
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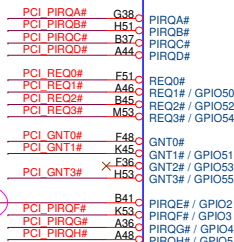
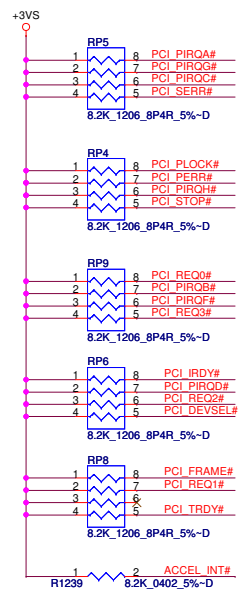
No used Integrated LAN,
connecting LAN_RST# to GND



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Size	Document Number	Rev		1.0	
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Sheet		17		of 49	



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						Size		Document Number		NAT02 M/B LA-5154P Schematic		Rev 1.0	
						Customer							
						Date							
								Thursday, November 26, 2009		Sheet		18 of 49	

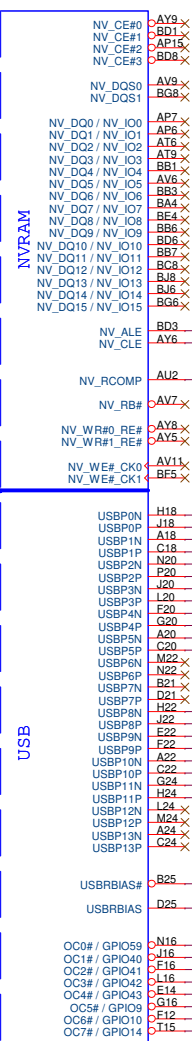


REV1.0

NVRAM

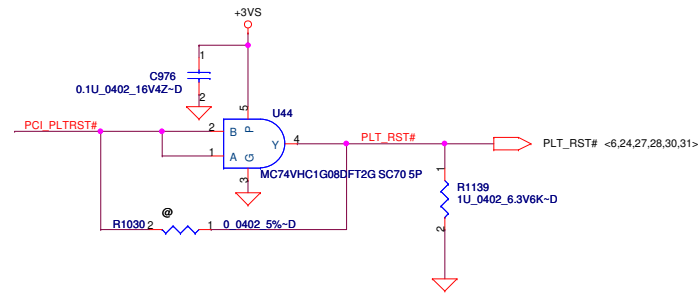
PCI

USB



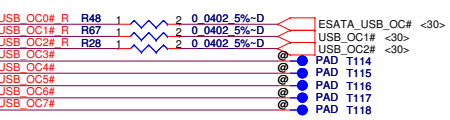
Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

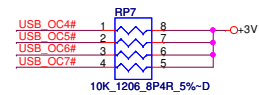
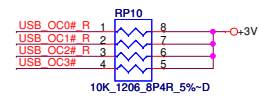


USB Port	Device
0	USB&ESATA
1	Reader board
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

From PCH EDS 5.18, USB port6 & 7 are not available in all sku.

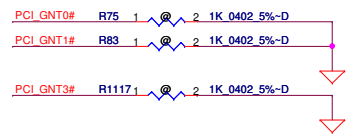


OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

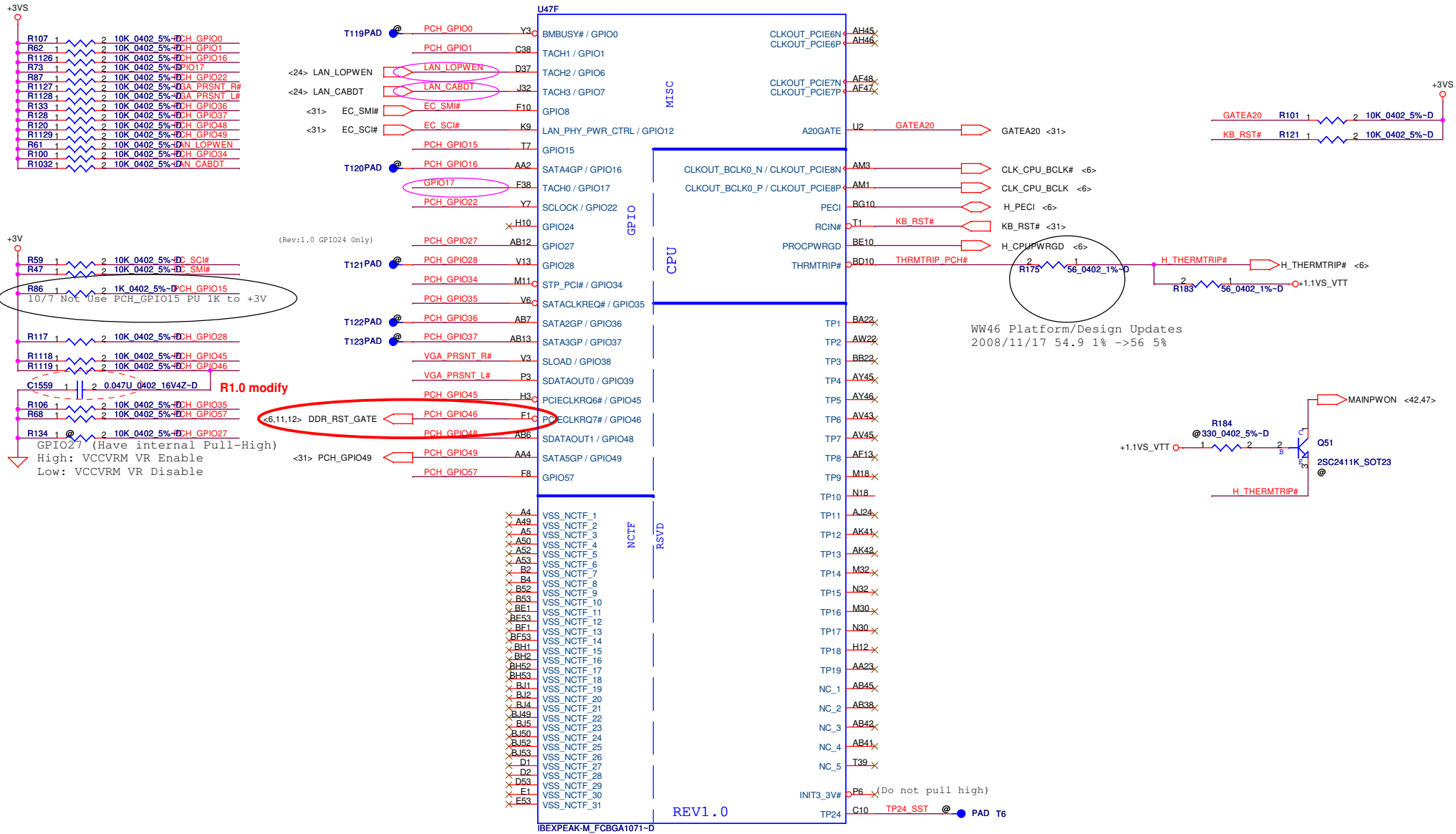


Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

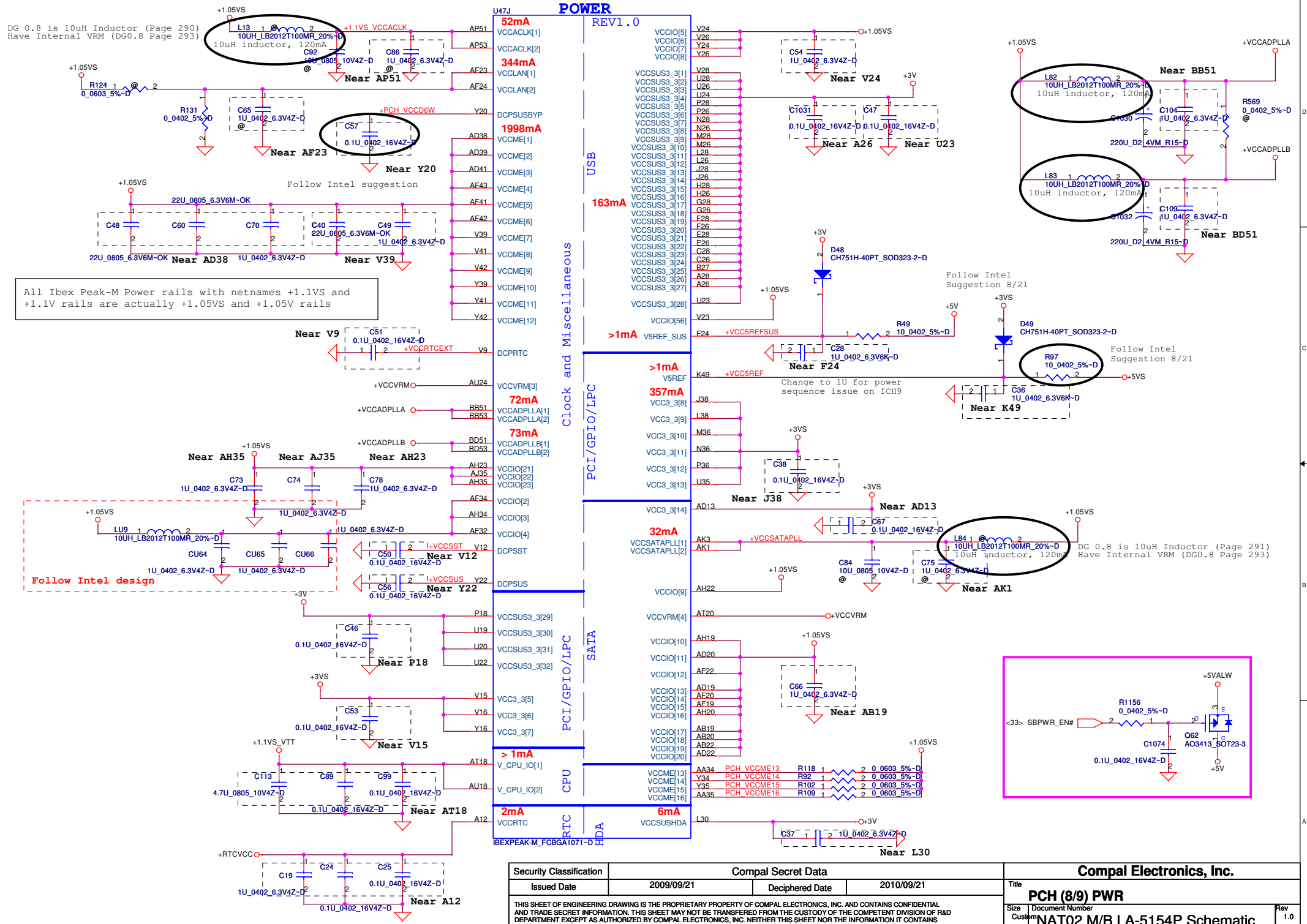
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



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				Customer	NAT02 M/B LA-5154P Schematic
				Date	Thursday, November 26, 2009
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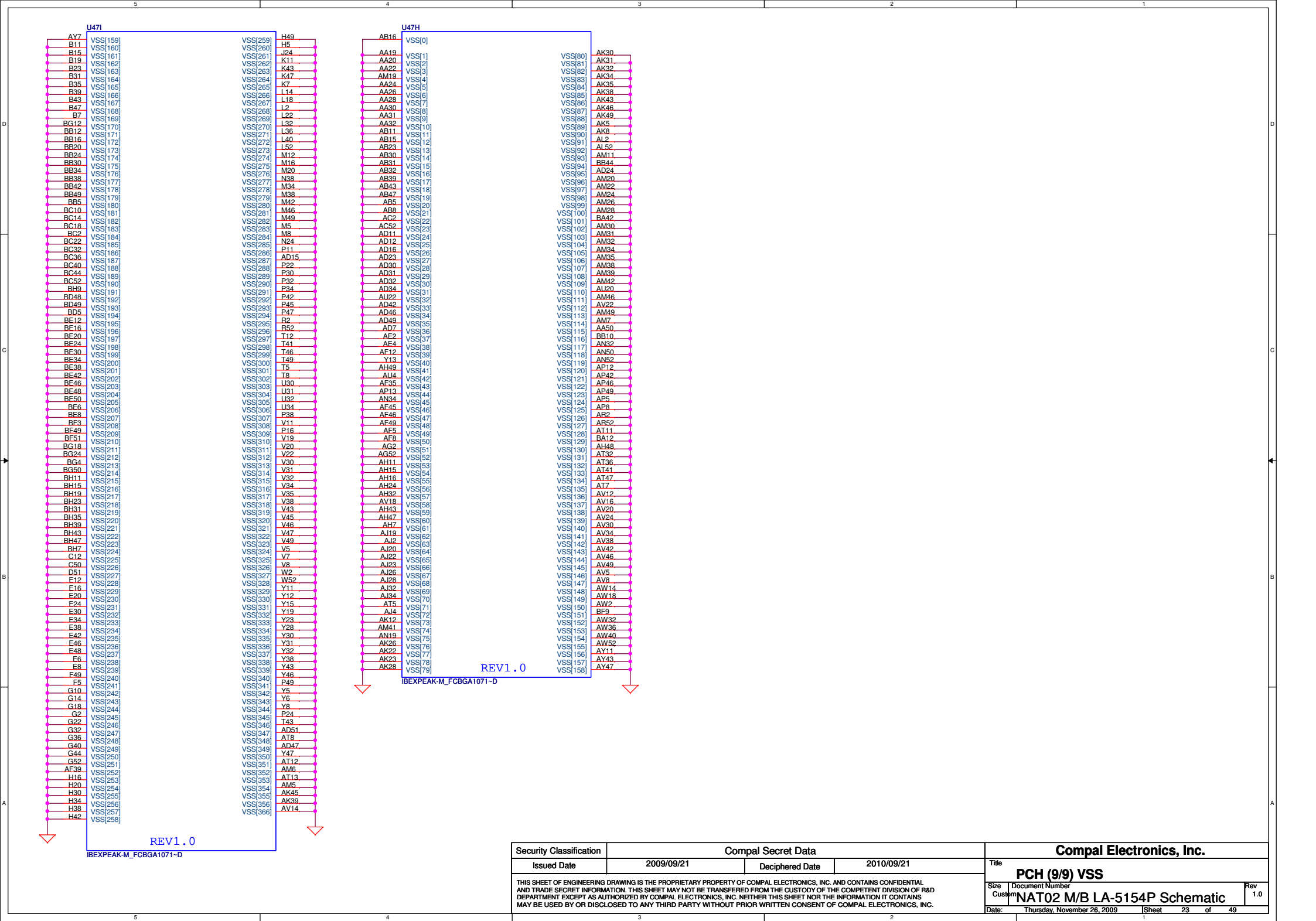


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Issued Date		2009/09/21		Deciphered Date		2010/09/21		Title	
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		Size		Document Number					Rev
		Customer		NAT02 M/B LA-5154P Schematic					1.0
		Date:		Thursday, November 26, 2009			Sheet		20 of 49

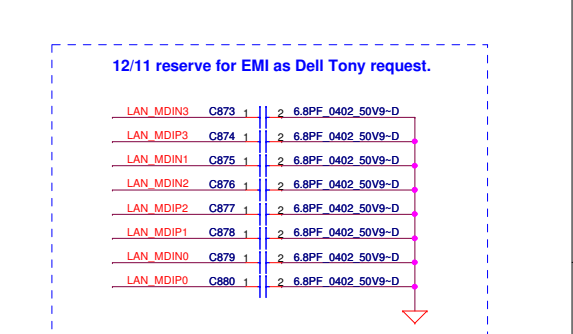
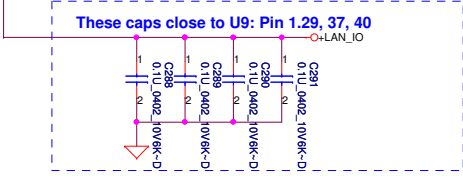
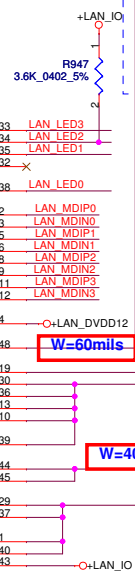
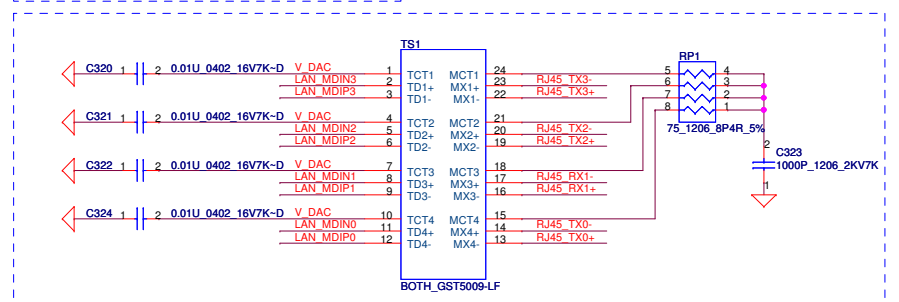


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Compal Electronics, Inc.			
Title			
PCH (8/9) PWR			
Size	Document Number		Rev
Custom	NAT02 M/B LA-5154P Schematic		1.0
Date:	Thursday, November 26, 2009	Sheet	22 of 49

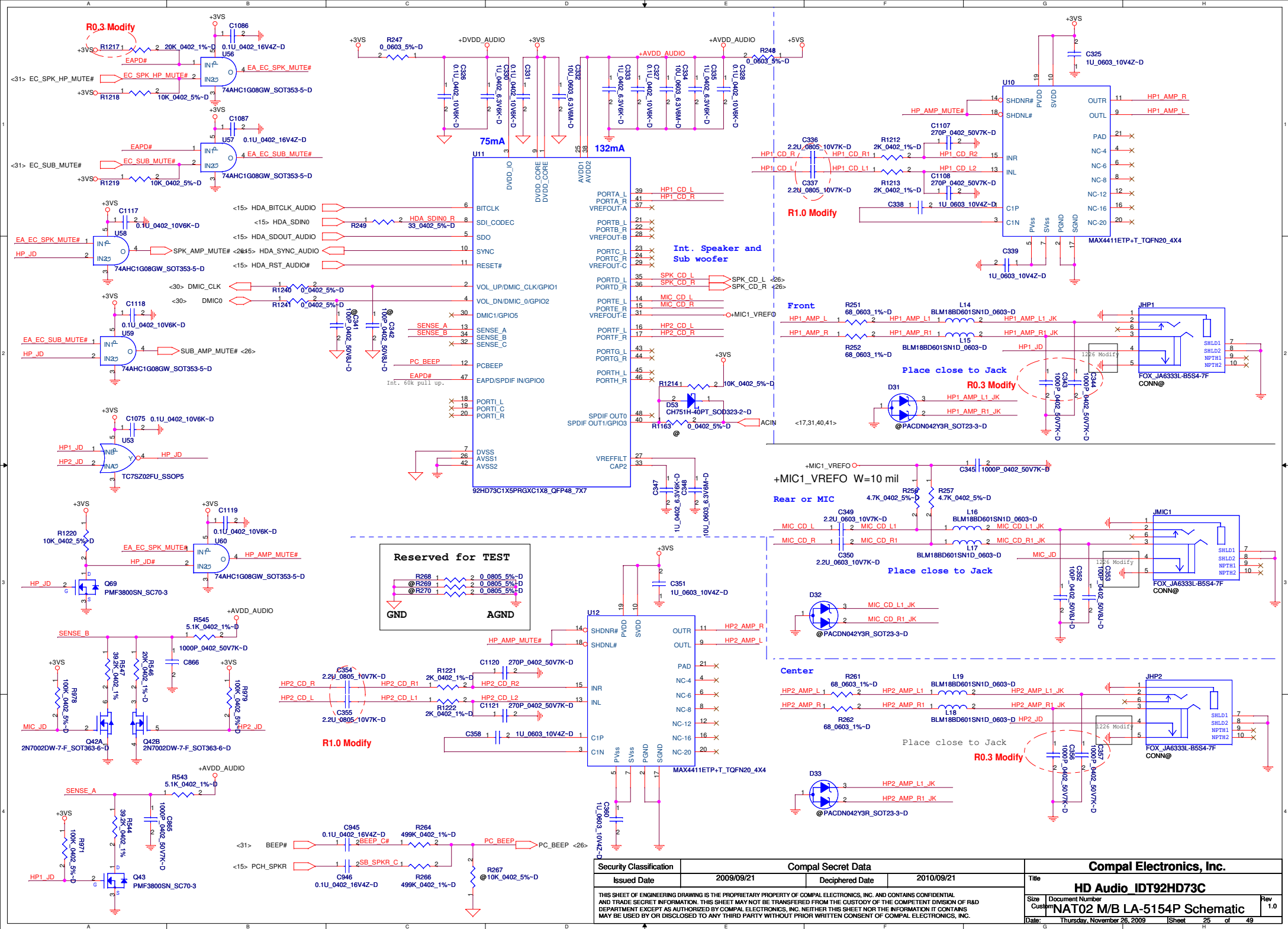


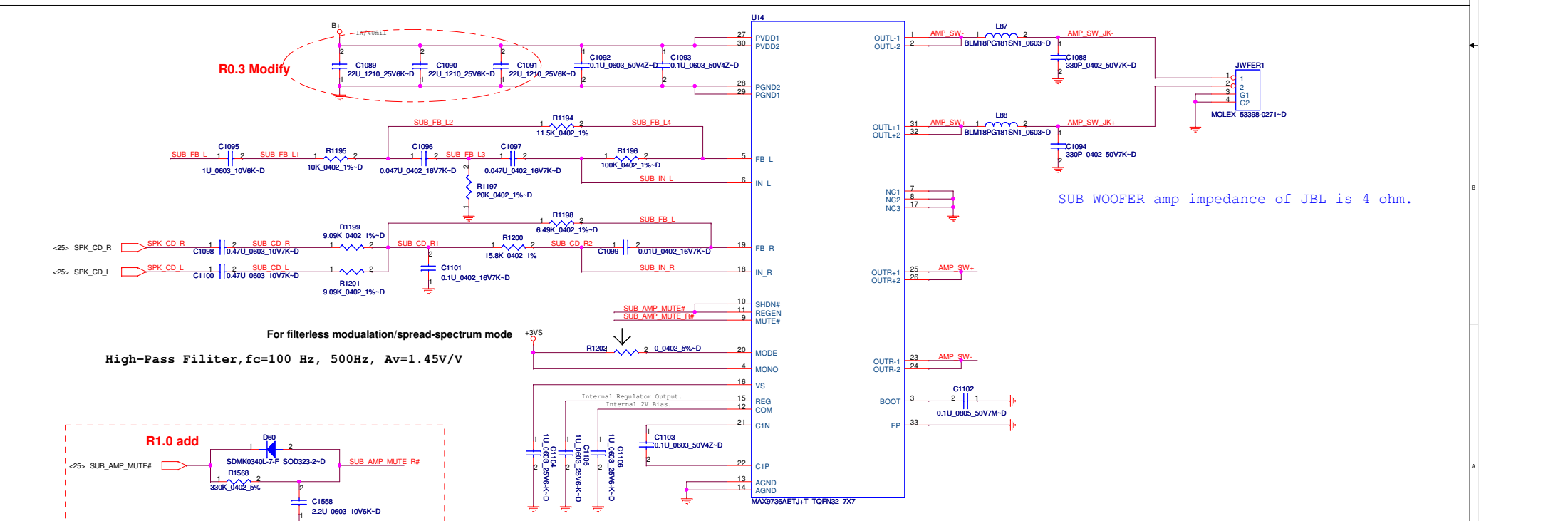
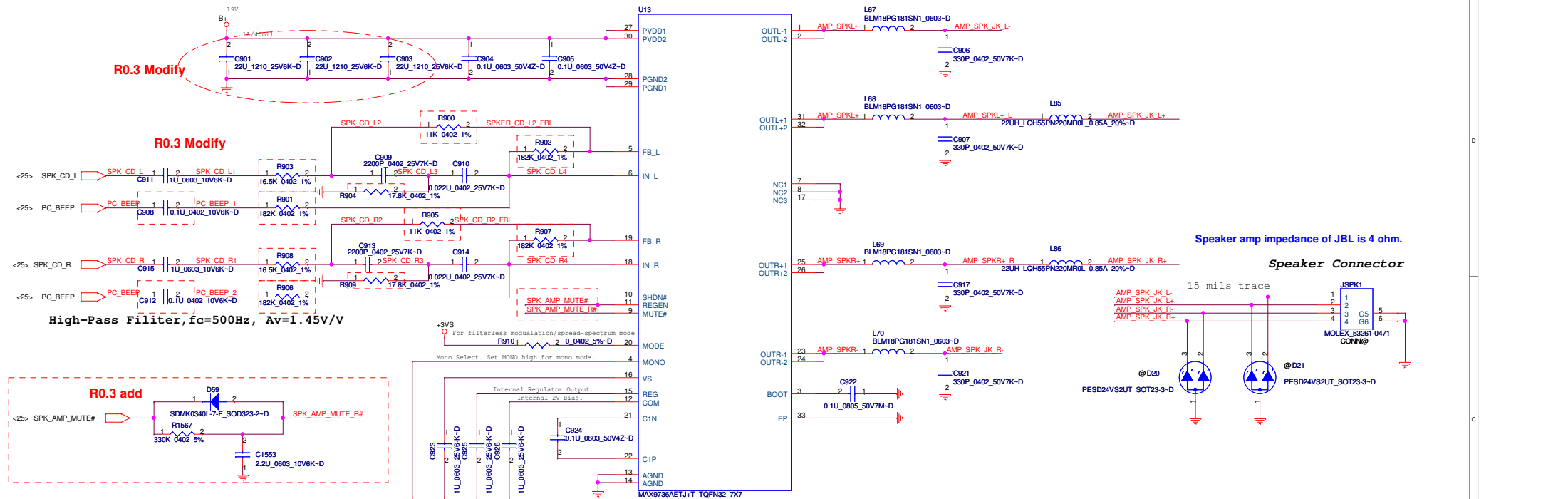
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date	2009/09/21		Deciphered Date	2010/09/21		Title					
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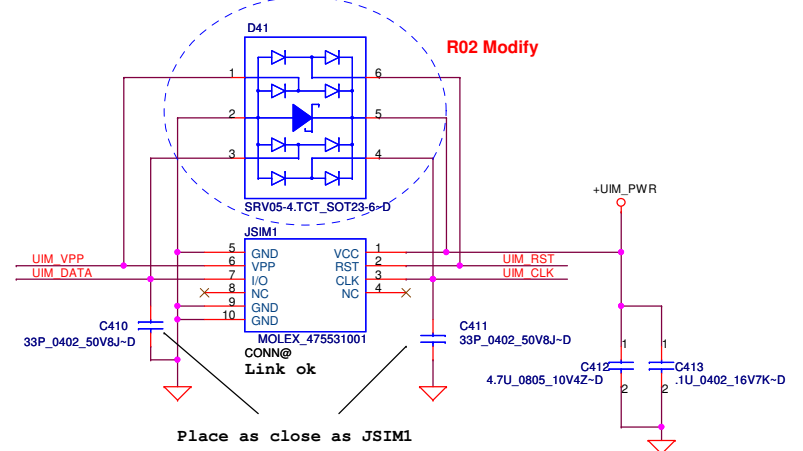
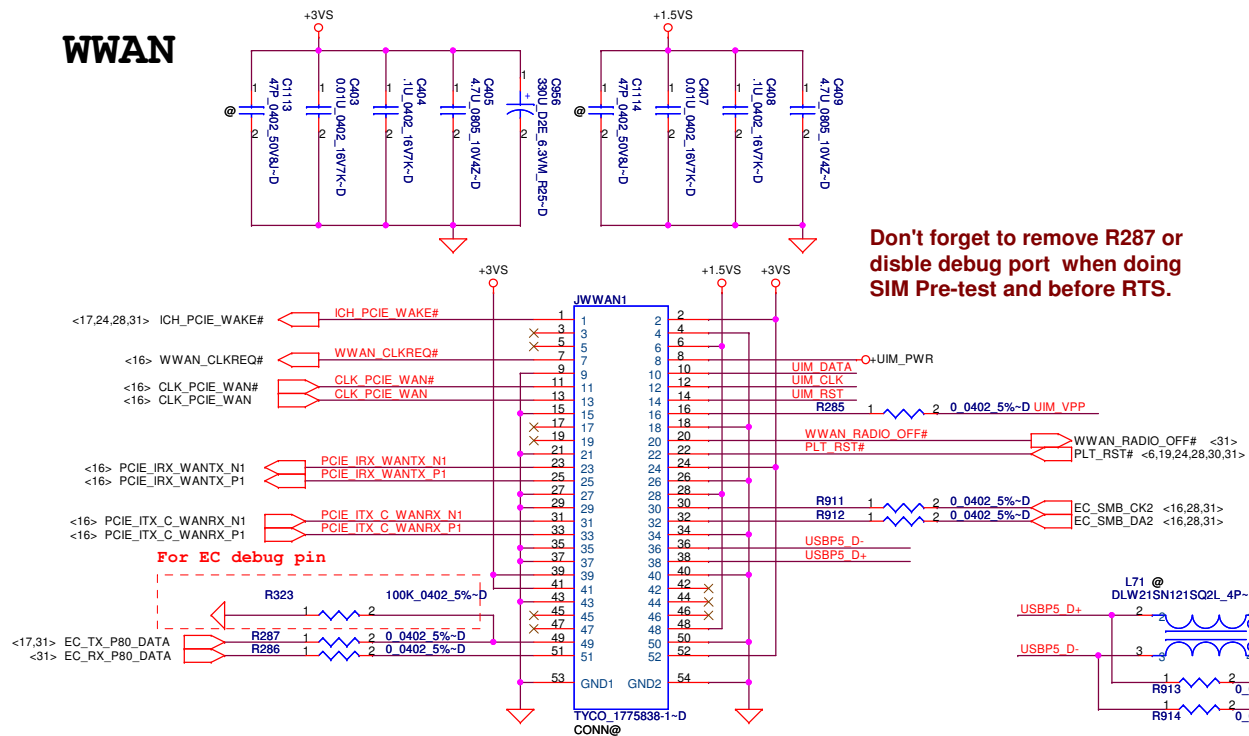
Compal Electronics, Inc.			
Title		Gigabit LAN RTL8111DL	
Size	Document Number		Rev
Customer	NAT02 M/B LA-5154P Schematic		1.0
Date:	Thursday, November 26, 2009	Sheet	24 of 49



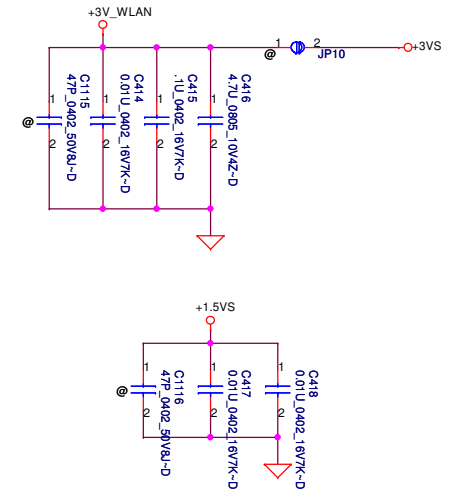
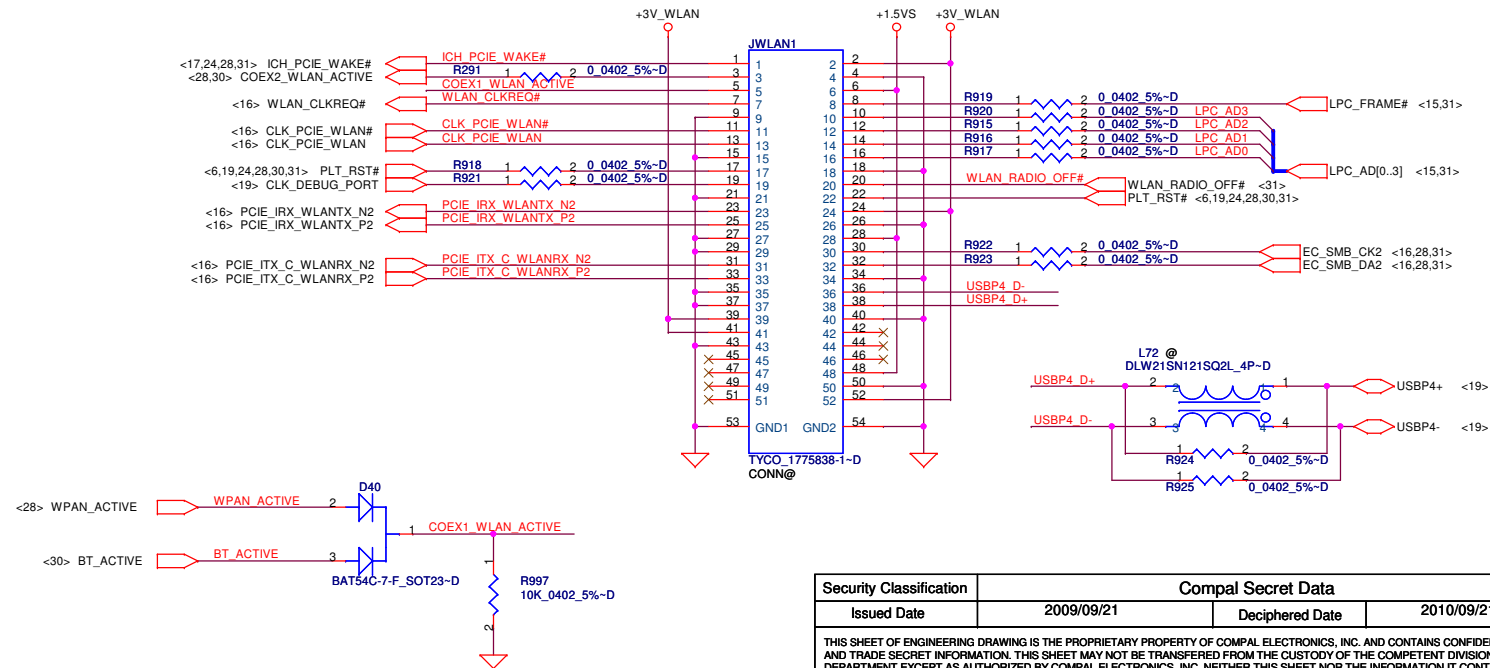


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				NAT02	M/B LA-5154P Schematic
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				Rev	1.0

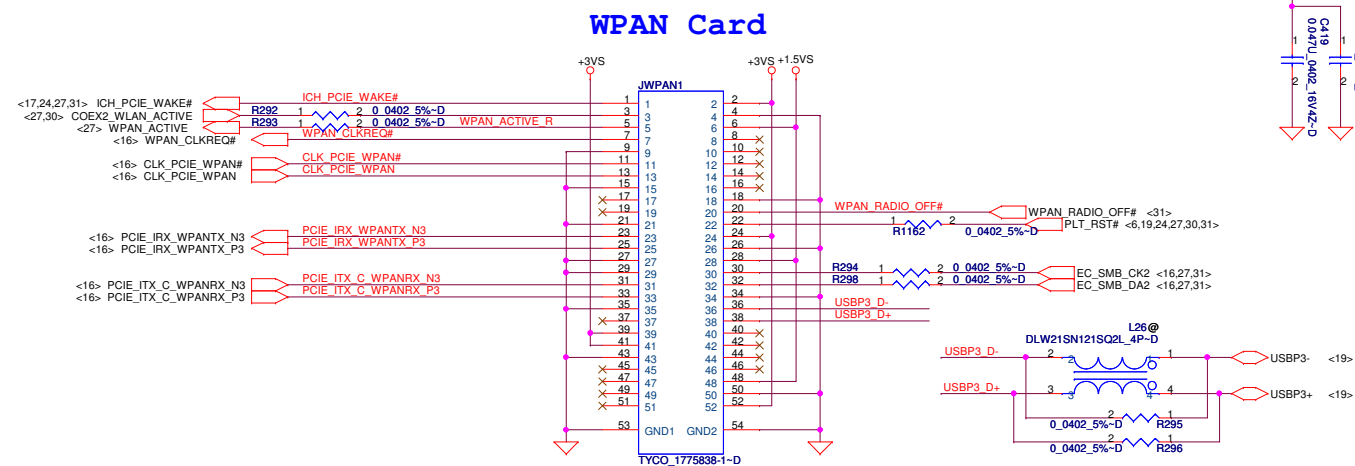
WWAN



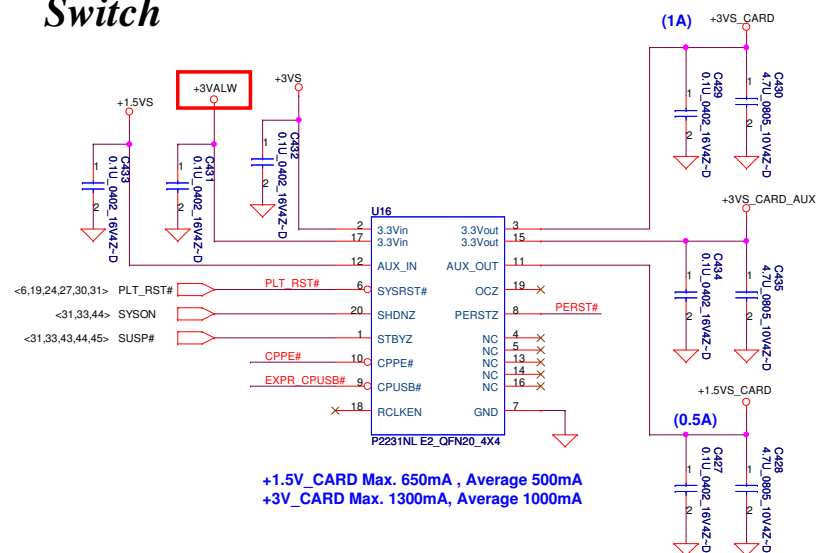
WLAN



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Issued Date	2009/09/21	Deciphered Date	2010/09/21	Title Mini Card_WLAN/WWAN	
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				Document Number	1.0
				Customer NAT02 M/B LA-5154P Schematic	
Date:		Thursday, November 26, 2009		Sheet	27 of 49

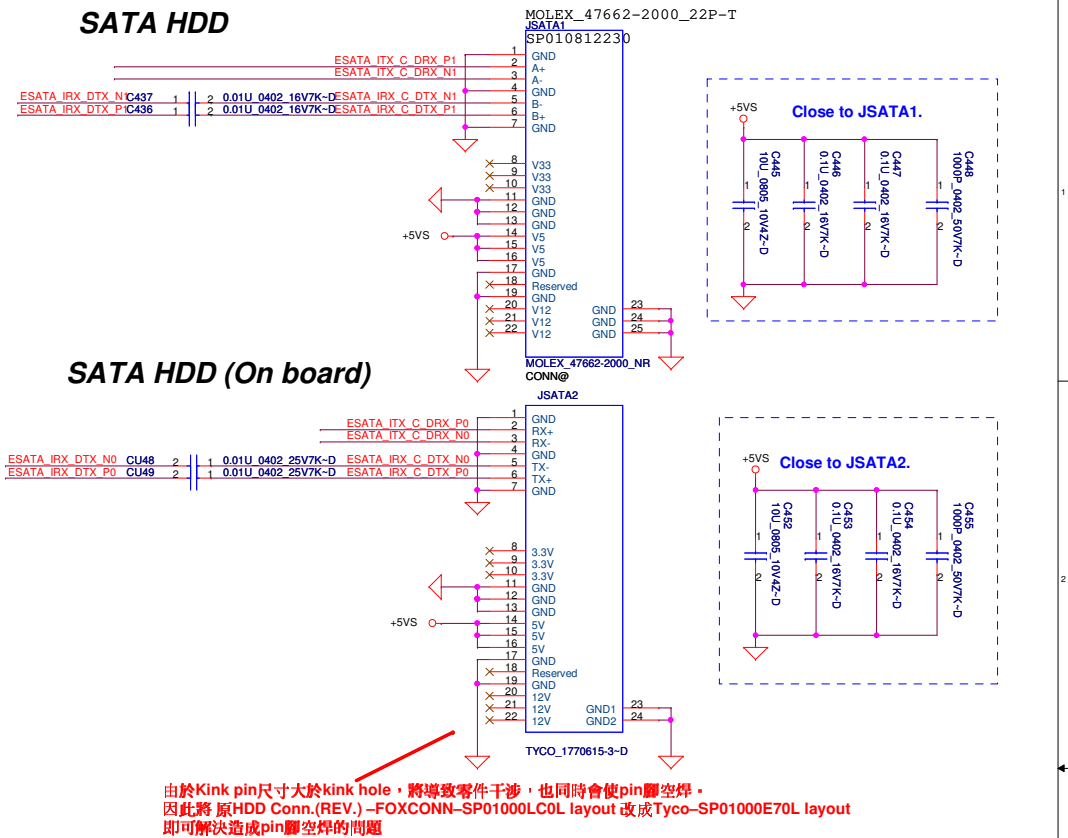


Express Card Power Switch

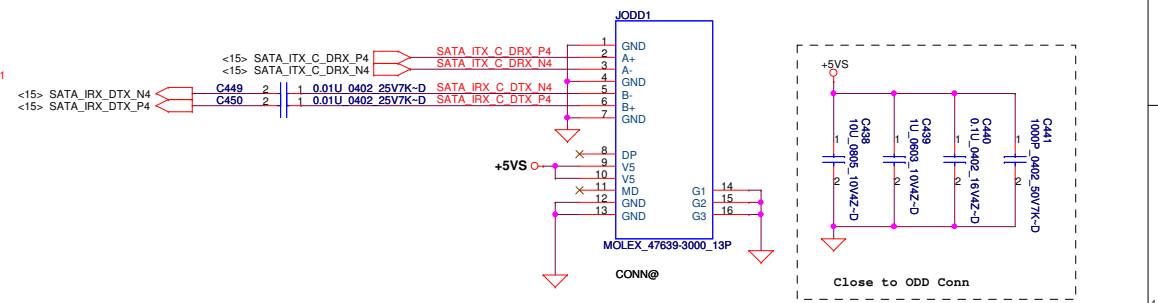


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				Size	Document Number
				NAT02 M/B LA-5154P Schematic	
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				Rev	1.0

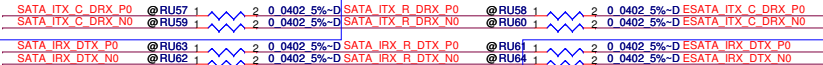
SATA HDD



SATA ODD CONN



Place close U67 pin 2 & pin3



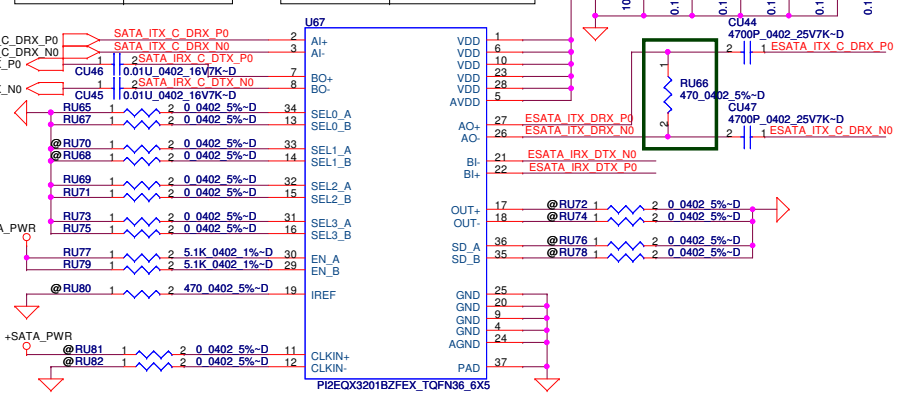
Place close U67 pin 21 & pin22

Output Swing Control

SEL2_ [A:B]	Swing
0	1x
1	1.2x

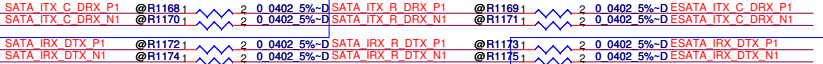
Output De-emphasis Adjustment

SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB

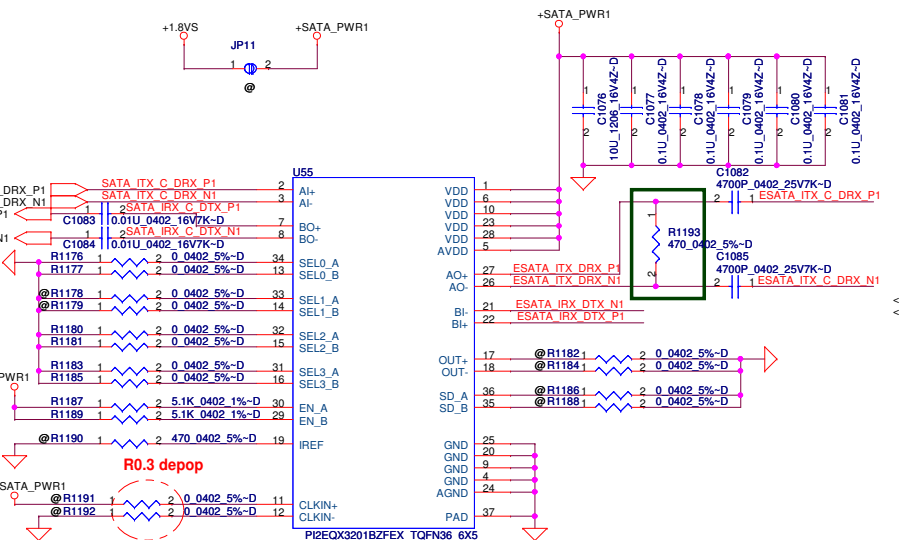


Place close U55 pin 2 & pin3

R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)



Place close U55 pin 21 & pin22



R0.3 depop

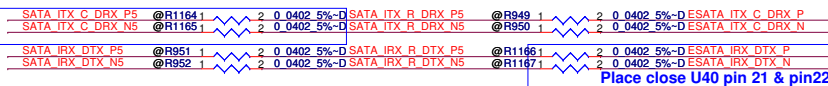
Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

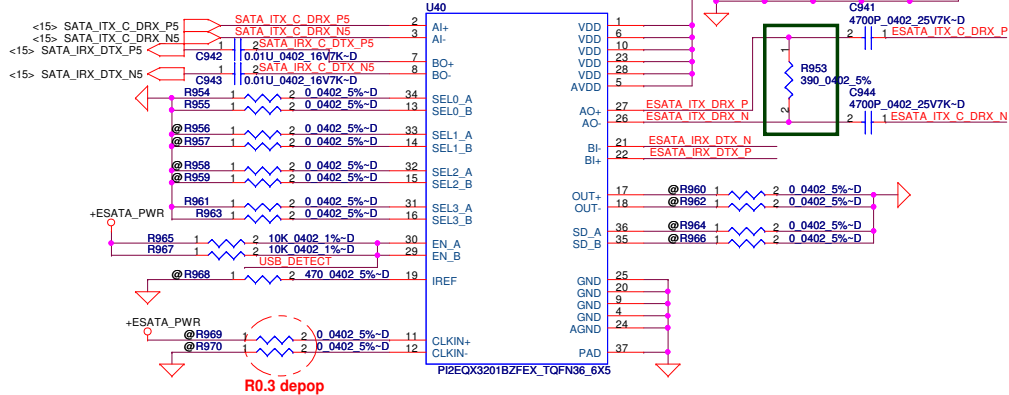
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		ODD/SATA HDD
Size	Document Number	Rev
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Place close U40 pin 2 & pin3



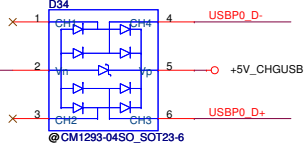
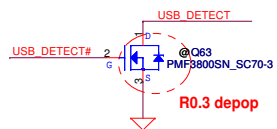
SEL2_ [A:B]	Swing
0	1x
1	1.2x

SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB

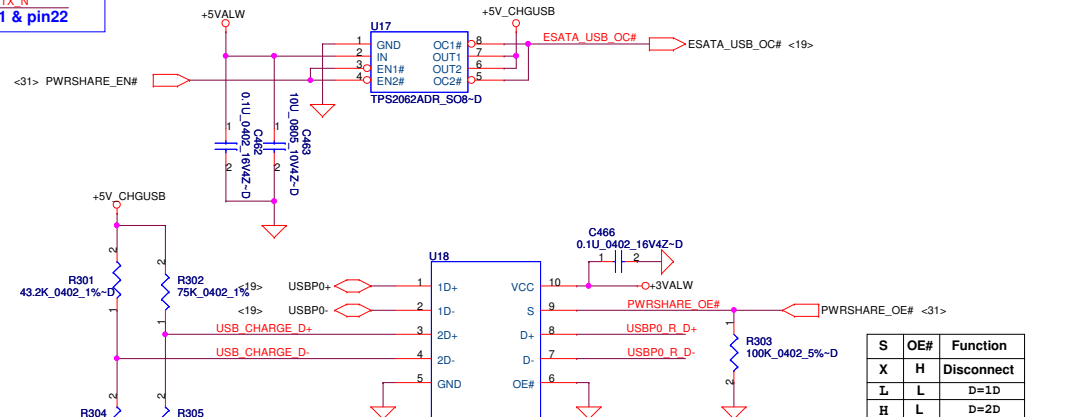


R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

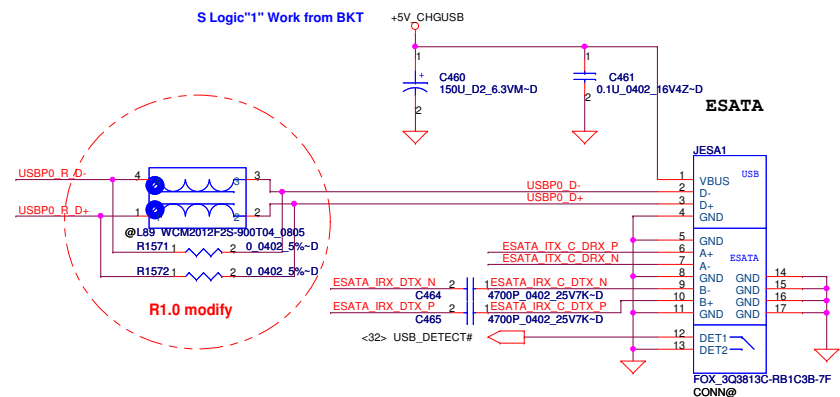
SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz



Place close JESA1



S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



ESATA

JESA1

USB

VBUS

D+

D-

GND

A+

A-

GND

B+

B-

GND

GND

GND

DET1

DET2

CONN@

FOX_303813C-RB1C3B-7F

CONN@

CONN@

CONN@

CONN@

CONN@

CONN@

CONN@

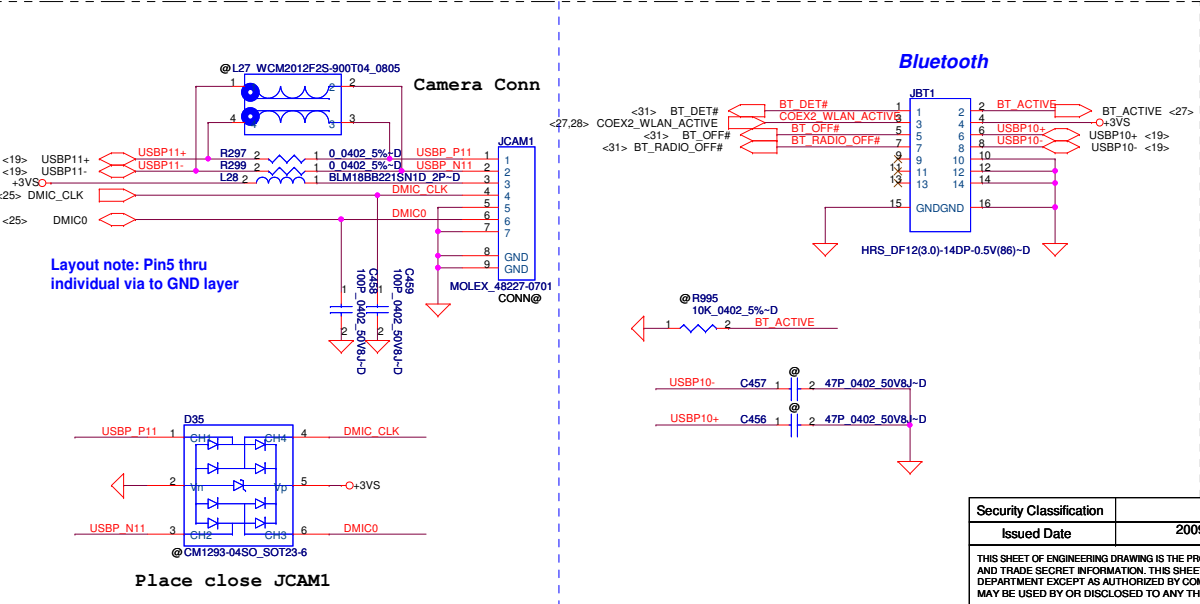
CONN@

CONN@

CONN@

CONN@

CONN@



Bluetooth

JBT1

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

BT_ACTIVE

Cardreader Connector

FOX_GS12301-1011A-9F-D

USB_EN#

USB_OC1#

USBP1+

USBP1-

USBP2+

USBP2-

USBP3+

USBP3-

USBP4+

USBP4-

USBP5+

USBP5-

USBP6+

USBP6-

USBP7+

USBP7-

USBP8+

USBP8-

to Single USB board

JSUSB1

USB2+

USB2-

USB3+

USB3-

USB4+

USB4-

USB5+

USB5-

USB6+

USB6-

USB7+

USB7-

USB8+

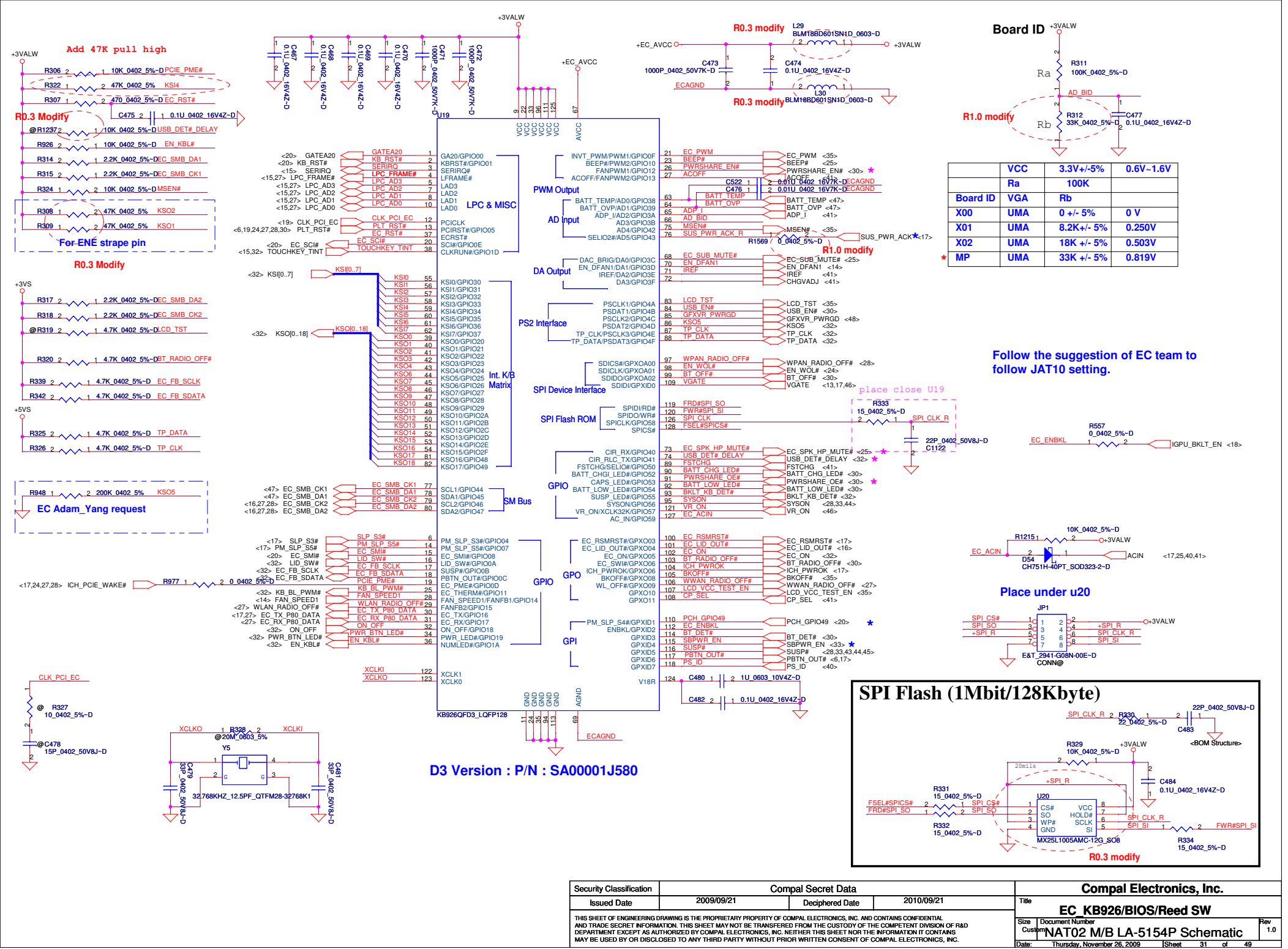
USB8-

USB9+

USB9-

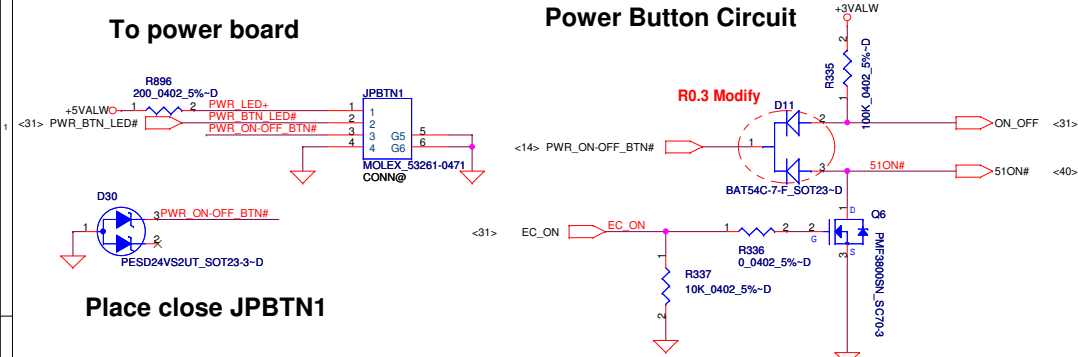
USB10+

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Title		
USB/BlueTooth/Camera/ESATA		
Size	Document Number	Rev
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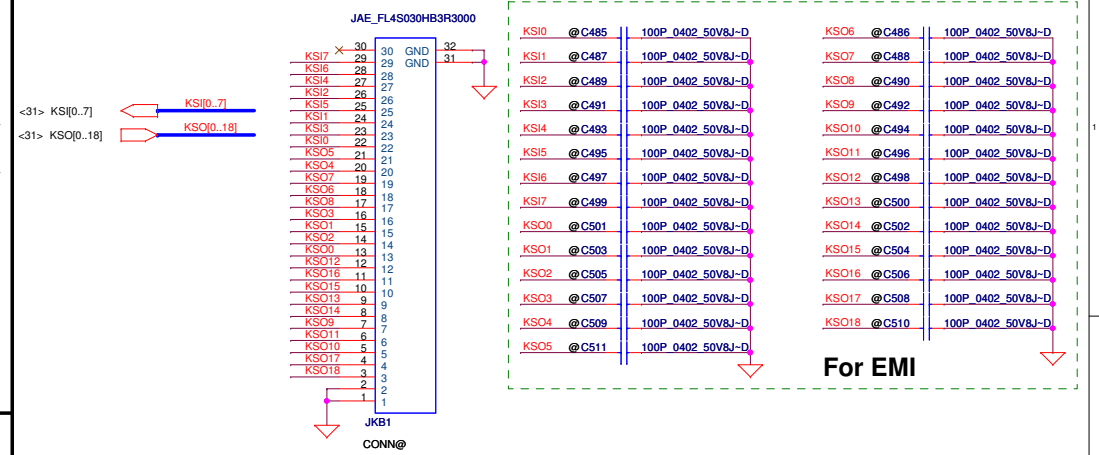
To power board

Power Button Circuit

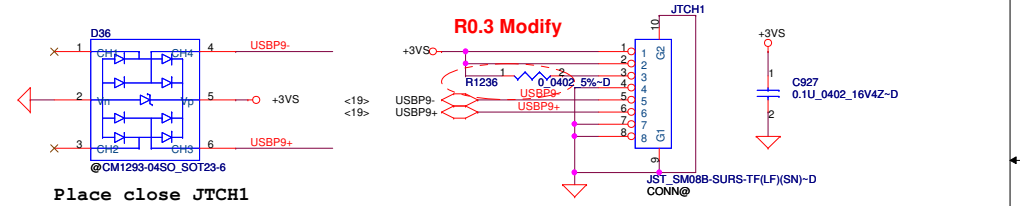


Place close JPBTN1

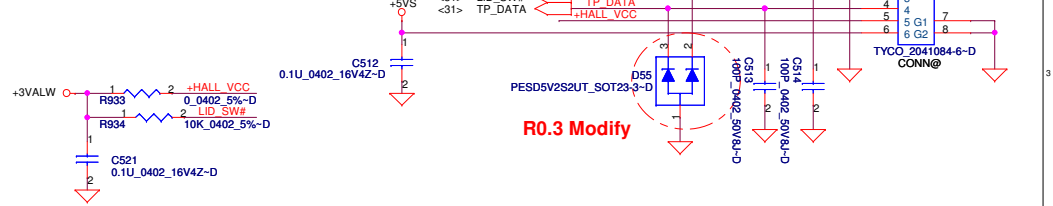
INT_KB_Conn.1



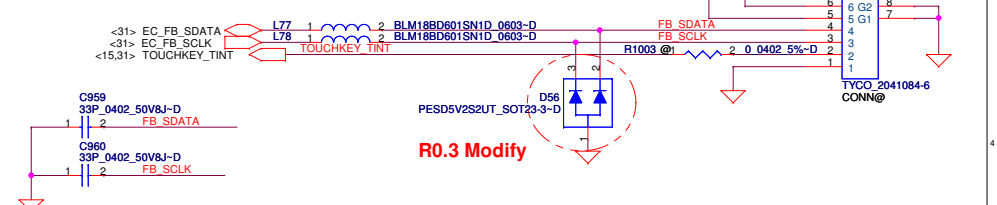
Touch Screen Connector



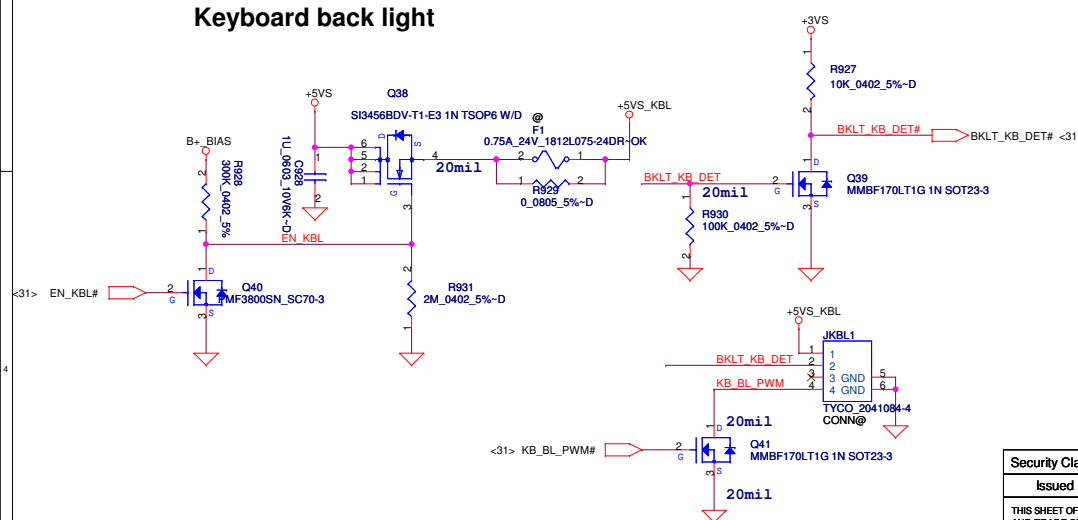
Touch PAD/B Conn.



Cap Sensor



Keyboard back light



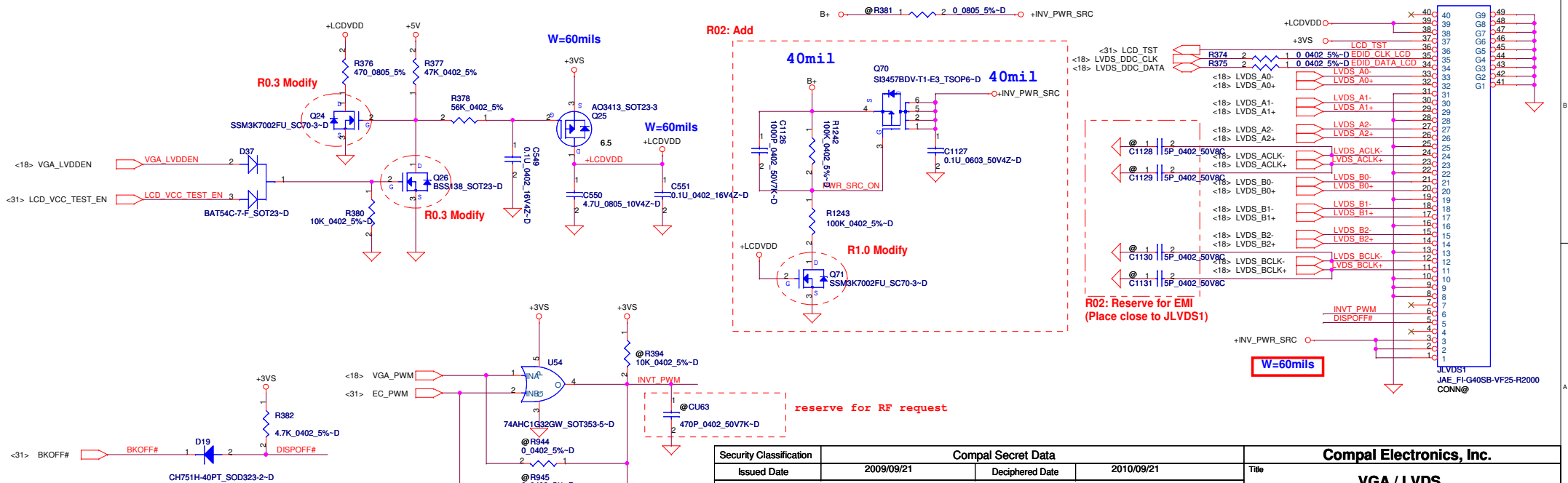
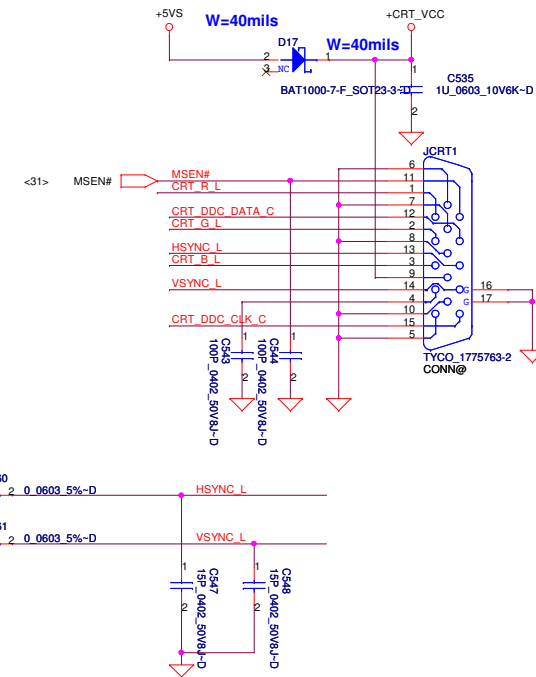
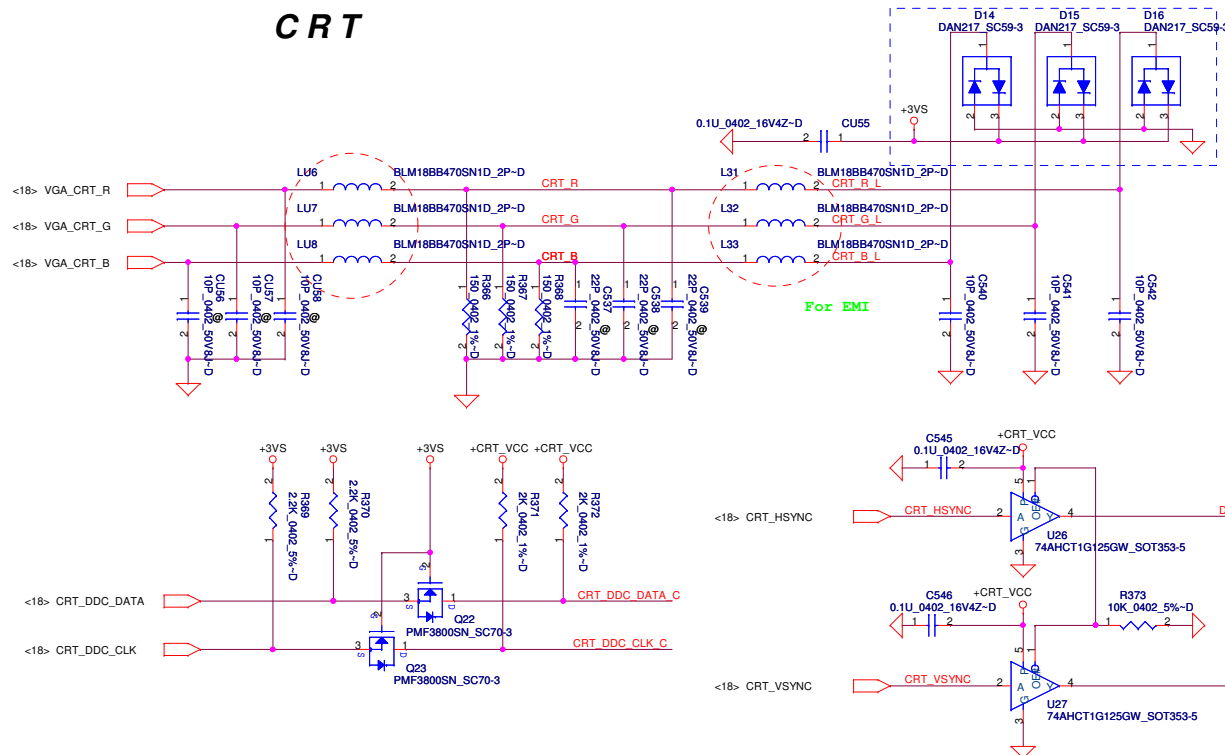
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/09/21				Title			
Deciphered Date				2010/09/21				PWROK/BTN/KB/Touch Pad			
Rev				1.0				NAT02 M/B LA-5154P Schematic			
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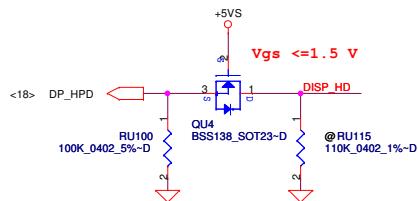
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Issued Date	2009/09/21	Deciphered Date	2010/09/21	Title	
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CRT



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				Deciphered Date				VGA / LVDS			
				2010/09/21				Size			
								Customer			
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								Rev			
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								Date			
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								35 of 49			

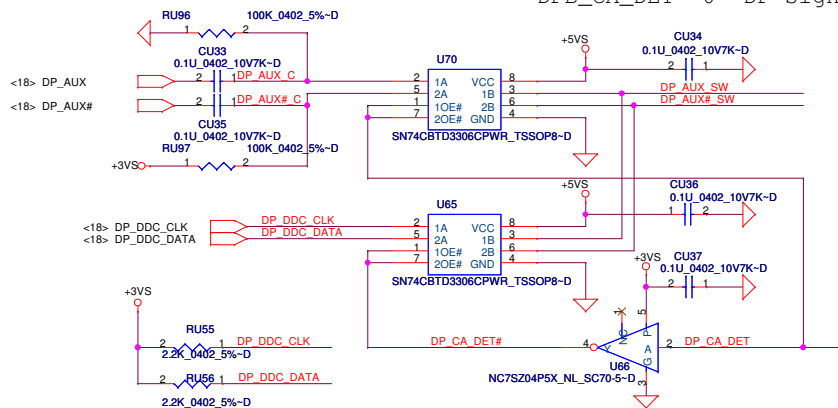
<18> DISP_A0N_VGA C561 2 1 0.1U 0402 10V6K-D DISP_A0N
 <18> DISP_A0P_VGA C562 2 1 0.1U 0402 10V6K-D DISP_A0P
 <18> DISP_A1N_VGA C563 2 1 0.1U 0402 10V6K-D DISP_A1N
 <18> DISP_A1P_VGA C564 2 1 0.1U 0402 10V6K-D DISP_A1P
 <18> DISP_A2N_VGA C566 2 1 0.1U 0402 10V6K-D DISP_A2N
 <18> DISP_A2P_VGA C568 2 1 0.1U 0402 10V6K-D DISP_A2P
 <18> DISP_A3N_VGA C569 2 1 0.1U 0402 10V6K-D DISP_A3N
 <18> DISP_A3P_VGA C570 2 1 0.1U 0402 10V6K-D DISP_A3P



Follow Intel HPD design rev 1.6

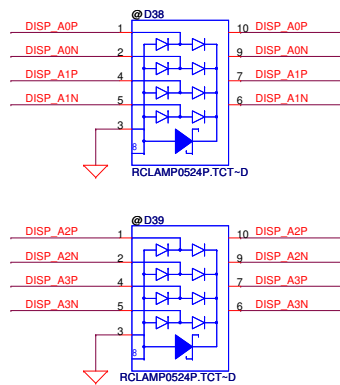
SW for MB side

DPB_CA_DET= 1 TMDs Signaling
 DPB_CA_DET= 0 DP Signaling

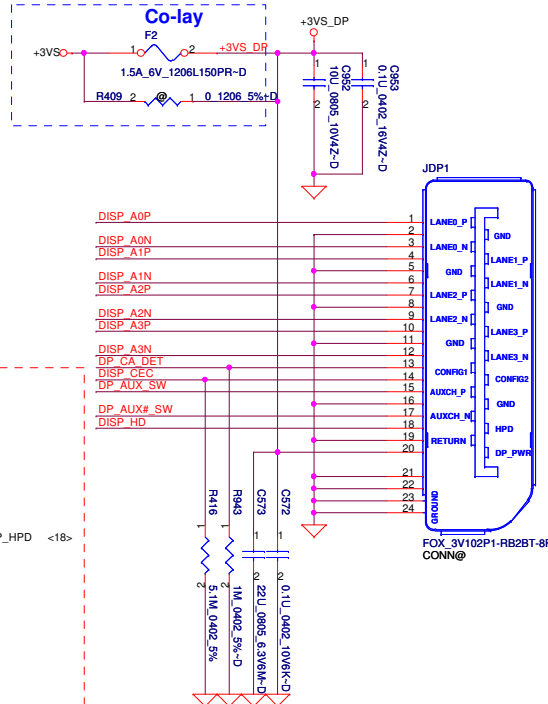


1225 modify it.

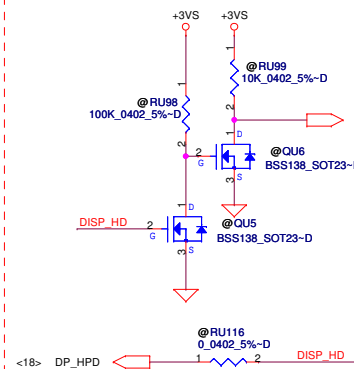
Place close JDP1



Co-lay



Reserve near connector



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				Deciphered Date				Display Port			
				2010/09/21				Size			
								Document Number			
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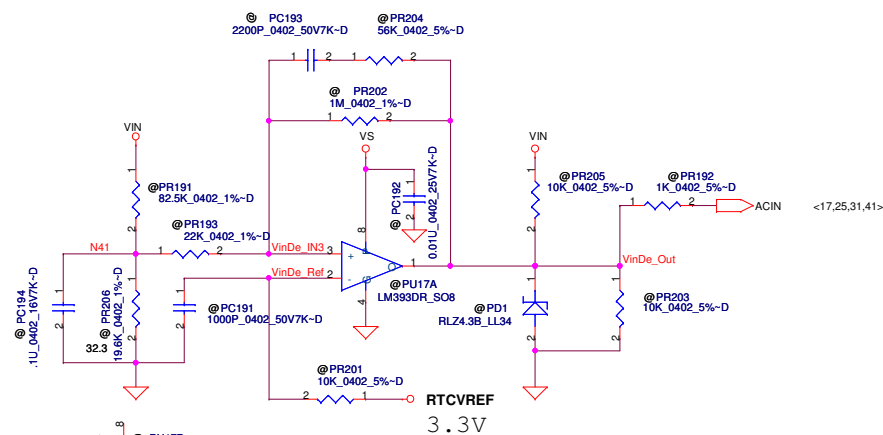
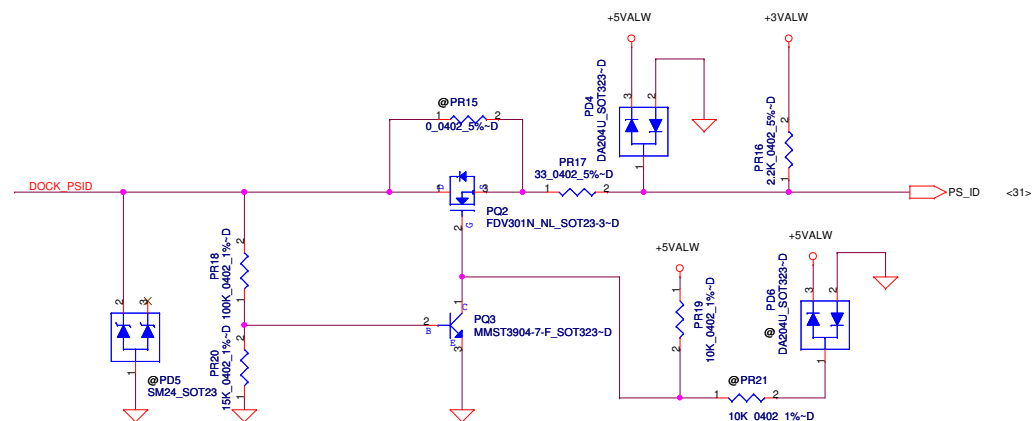
Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	08	PROCESSOR (4/6) PWR,Bypass	2009/07/22	Compal	Design change for IMVP6.5 current gain	R343 un-pop,R1072 pop,R1074 pop,R1073 unpop,R1075 pop,R1076 un-pop	Rev02 (X01)
02	16	PCH (2/9) PCIE, SMBUS, CLK	2009/08/10	Compal	XTAL25_IN should be pulled to GND using a 0Q resistor.	Pop C1027 with a 0 ohm resister	Rev02 (X01)
03	06	+1.5V and reseret	2009/08/10	Compal	Reduce S3 state Power	Add U63,Q36,R290,R310,R1103,R1136,C1142	Rev02 (X01)
04	09	Separate +1.5V power	2009/08/10	Compal	Reduce S3 state Power	Add PJP12,PJP13,PJP14,C1033,C1143,C1144,C1145	Rev02 (X01)
05	11	VrefDQ	2009/08/10	Compal	VrefDQ should be Maintained within SPEC during S3	Add Q37,R313	Rev02 (X01)
06	12	VrefDQ	2009/08/10	Compal	VrefDQ should be Maintained within SPEC during S3	Add Q44,R321	Rev02 (X01)
07	20	DDR_RST_GATE	2009/08/10	Compal	DDR_RST_GATE from GPIO46	Add GPIO46	Rev02 (X01)
08	33	VDDQ	2009/08/10	Compal	Processor VDDQ should be turned off in S3	Add Q73,Q11,R346,R349,R1158,C534,C536	Rev02 (X01)
09	15	GPIO1D	2009/08/18	Compal	ADD EC GPIO1D to PCH GPIO33	Add GPIO33	Rev02 (X01)
10	26	Sub woofer / Speaker AMP	2009/08/25	Compal	Reserve Subwoofer delay circuit for mute	Reserve D60, R1568, C1558	Rev02 (X01)
11	24,31		2009/08/25	Compal	Follow crystal vendor's recommend	C318,C319,C479,C481 BOM change to SE071330J8L (S CER CAP 33P 50V +-5% NPO 0402)	Rev02 (X01)
12	6	PROCESSOR (2/6) CLK,JTAG	2009/08/25	Compal	Intel S3 solution disable	POP R1054,R1055,R1121; Depop Q36,R290,R1103	Rev02 (X01)
13	11,12		2009/08/25	Compal	Intel S3 solution disable	Depop Q37,Q44,R56	Rev02 (X01)
14	33	DC/DC Interface	2009/08/25	Compal	Intel S3 solution disable	Depop Q73 Q73 BOM change to SB0000001Y8L R358 BOM change to SD013470080 (S RES 1/10W 470 +-5% 0603)	Rev02 (X01)
15	35	VGA / LVDS	2009/08/25	Compal	to improve +LCDVDD voltage quality.	Pop C550	Rev02 (X01)
16	31	EC_KB926/BIOS/Reed SW	2009/08/25	Compal	Board ID change	R312 BOM change to 8.2K	Rev02 (X01)
17	31	EC_KB926/BIOS/Reed SW	2009/08/25	Compal	Reserve a 0ohm resister on SUS_PWR_ACK from PCH to EC	Reserve R1569 on SUS_PWR_ACK	Rev02 (X01)
18	35		2009/09/01	Compal	In common with MV	Q71 BOM change to SB000000960L	Rev02 (X01)
19	20		2009/09/21	Compal	S3 POWER Reduction update from Intel	Reserve C1559 on DDR_RST_GATE	Rev03 (X02)
20	30		2009/09/21	Compal	Reserve common choke on USB0	Reserve L89,R1571,R1572	Rev03 (X02)

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				Size	Document Number	Rev
				Custom	NAT02 M/B LA-5154P Schematic	1.0
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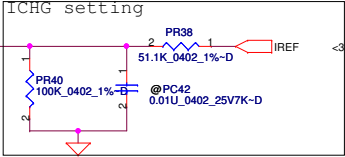
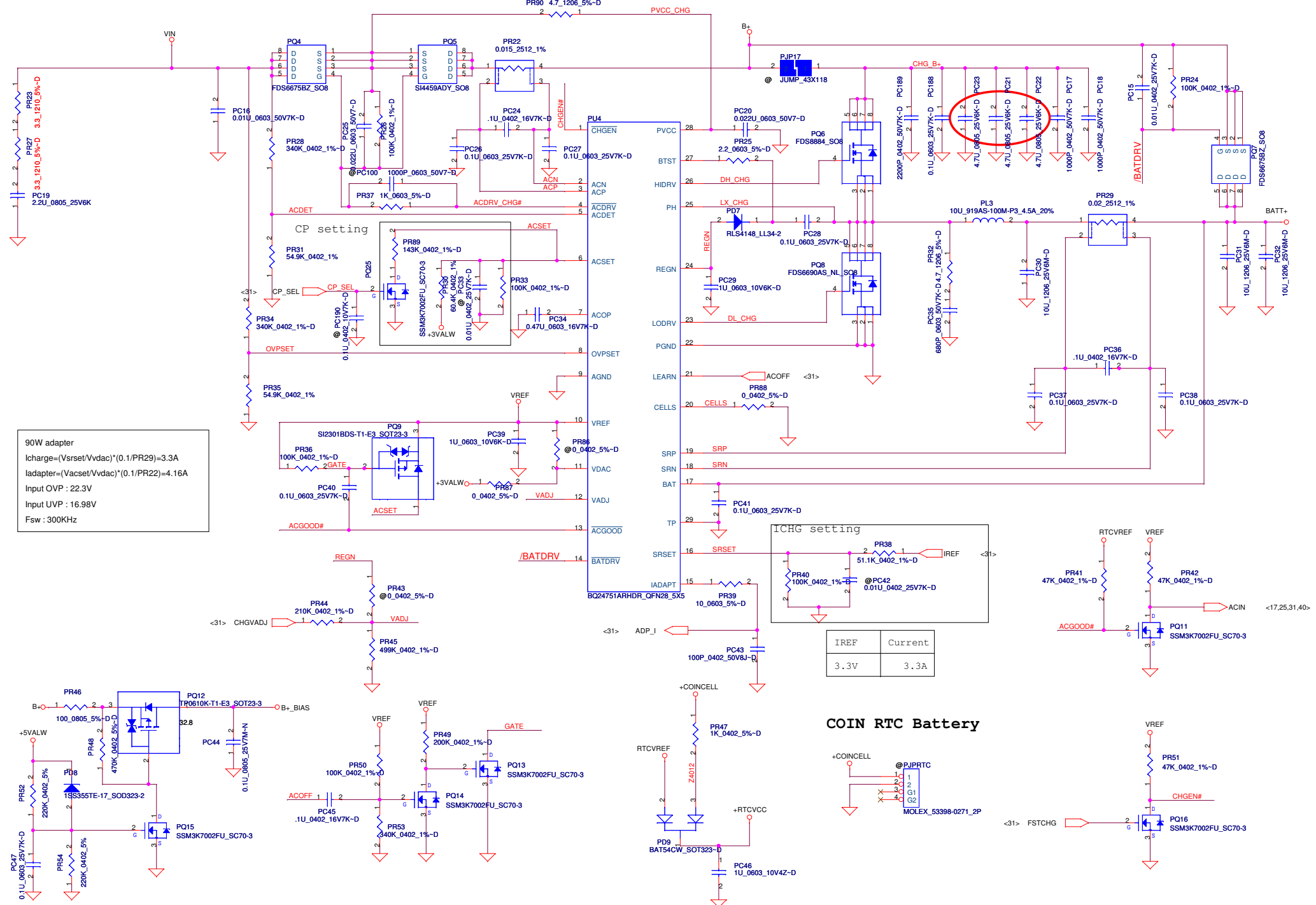
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	30	ESATA	2009/09/21	Compal	Add ESATA re-driver	Unpop R1164,R1165,R1166,R1167,R949,R950,R951,R952 pop JP13,C941,C944,C942,C943	Rev03 (X02)
02	33		2009/09/21	Compal		Q55,Q73 BOM change to SB00000DA0L	Rev03 (X02)
03	8		2009/09/21	Compal	BOM reason	C1009,C1010 BOM change to SGA00002U1L	Rev03 (X02)
04	25	HD Audio_IDT92HD73C	2009/09/21	Compal		BOM change for C336,C337,C354,C355	Rev03 (X02)
05	26	Sub woofer/Speaker AMP	2009/09/21	Compal	implement Subwoofer delay circuit for mute	Pop D60,C1558 R1568 change to 330K	Rev03 (X02)
06	37	Display Port	2009/09/21	Compal	Follow Intel HPD design	remove RU98,RU99;add RU115; change QU4 to SB50138008L	Rev03 (X02)
07	22	PCH (8/9) PWR	2009/09/21	Compal	Follow Intel design	Add LU9,CU64,CU65,CU66	Rev03 (X02)
08	11, 12	DDRIII SO-DIMM	2009/10/08	Compal	Add M3 solution	Pop R166,R178	Rev03 (X02)
09	31	EC	2009/10/12	Compal	For ENE issue	Add R322 47K ohm pull high	Rev03 (X02)
10	17	PCH	2009/10/15	Compal	Bom reason	Change U2 SA007080B90 to SA007080100	Rev03 (X02)
11	19	PCH	2009/10/16	Compal	Design follow NAT01	Change R1139 SD02810038L to SE000000K8L	Rev03 (X02)
12	31	EC	2009/10/22	Compal	Change Board ID	Change R312 SD02882018L to SD02818028L	Rev03 (X02)
13	32	Touch Screen	2009/11/02	Compal	Add for Touch Screen issue	Add R1236	Rev03 (X02)
14	36	HDMI	2009/11/24	Compal	For HDMI Deep color mode	Unpop RU28,RU32 , Pop RU30,RU33	Rev10 (A00)
15	30	Camera	2009/11/02	Compal	improve 888MHZ noise	Add C458,C459	Rev10 (A00)
16	27	WLAN	2009/11/05	Compal	for EC debug pin	Add R323 100K pull down	Rev10 (A00)
17	9	PWR	2009/11/05	Compal	Intel suggest to reduce GFX voltage overshoot	Change RU93 to 470ohm	Rev10 (A00)
18	26	Sub woofer/Speaker Amp	2009/11/16	Compal	Follow NAT01 design	Change C922 & C1102 to 0.1uF	Rev10 (A00)
19	31	EC	2009/11/19	Compal	Change Board ID	Change R312 SD02818028L to SD02833028L	Rev10 (A00)
20	36	HDMI	2009/11/24	Compal	Change HDMI level shift	Change U63 to SA00003GT00	Rev10 (A00)
21	36	HDMI	2009/11/24	Compal	For HDMI Deep color mode	Add RU25 4.7K pull down for ASM1442	Rev10 (A00)
22	36	HDMI	2009/11/24	Compal	For HDMI Deep color mode	Reserve RU37 4.7K pull high for ASM1442	Rev10 (A00)
23	36	HDMI	2009/11/24	Compal	For HDMI Level shift ASM1442	Change RU29 to 3.4K for ASM1442	Rev10 (A00)
24							
25							

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				Size	Document Number	Rev
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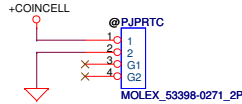
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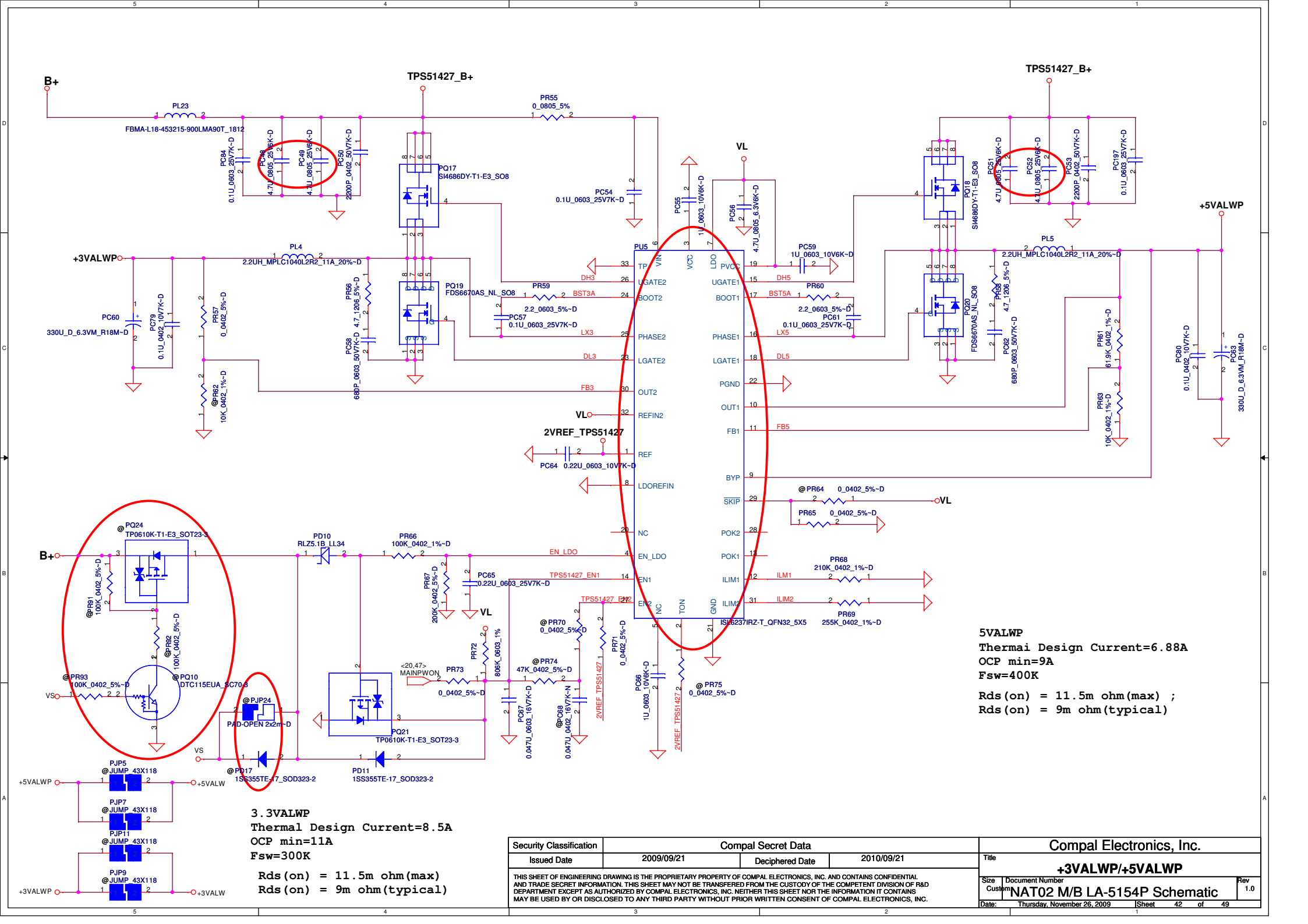
90W adapter
 $I_{charge} = (V_{rsrset}/V_{vdac}) * (0.1/PR29) = 3.3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR22) = 4.16A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



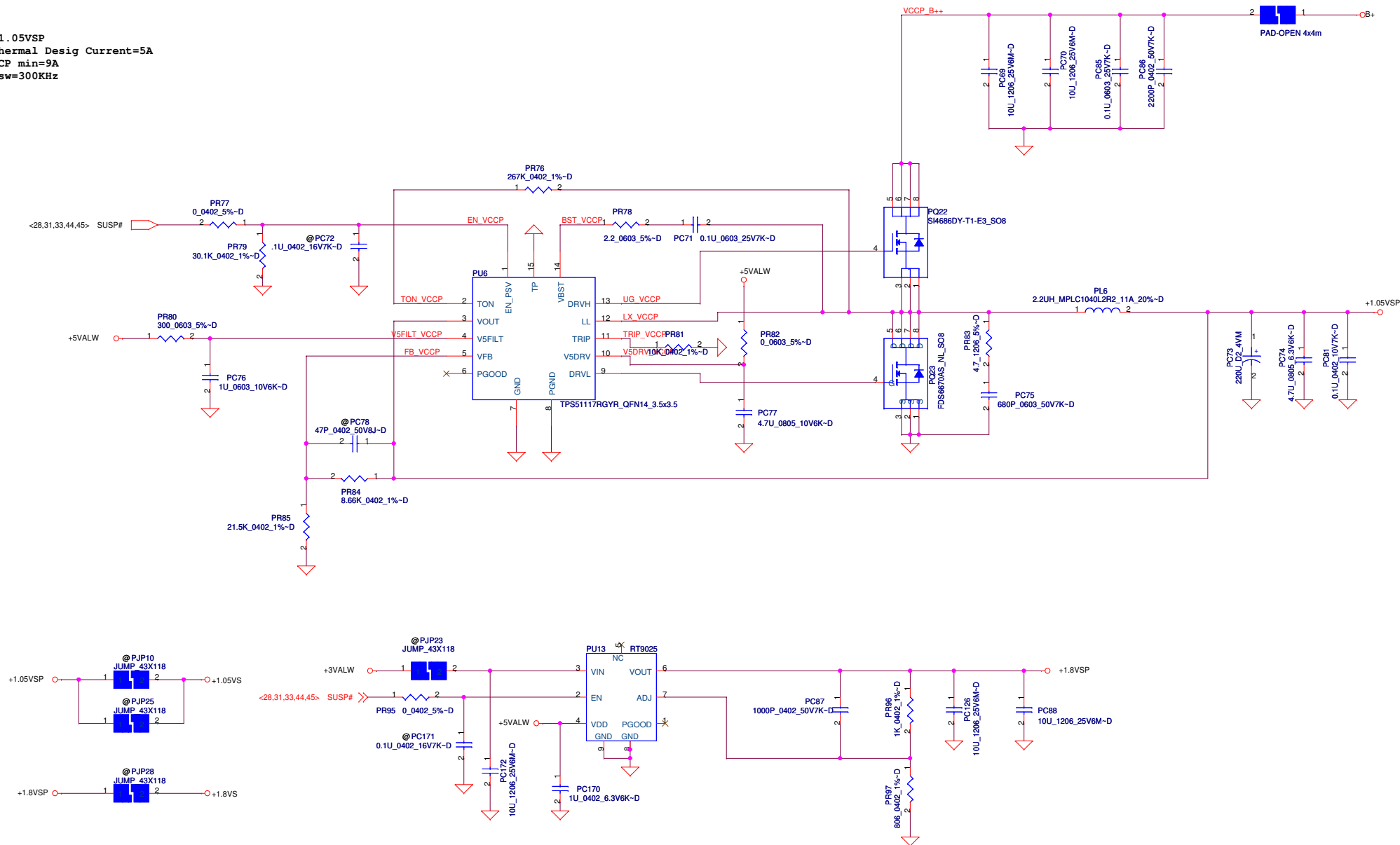
IREF	Current
3.3V	3.3A

COIN RTC Battery



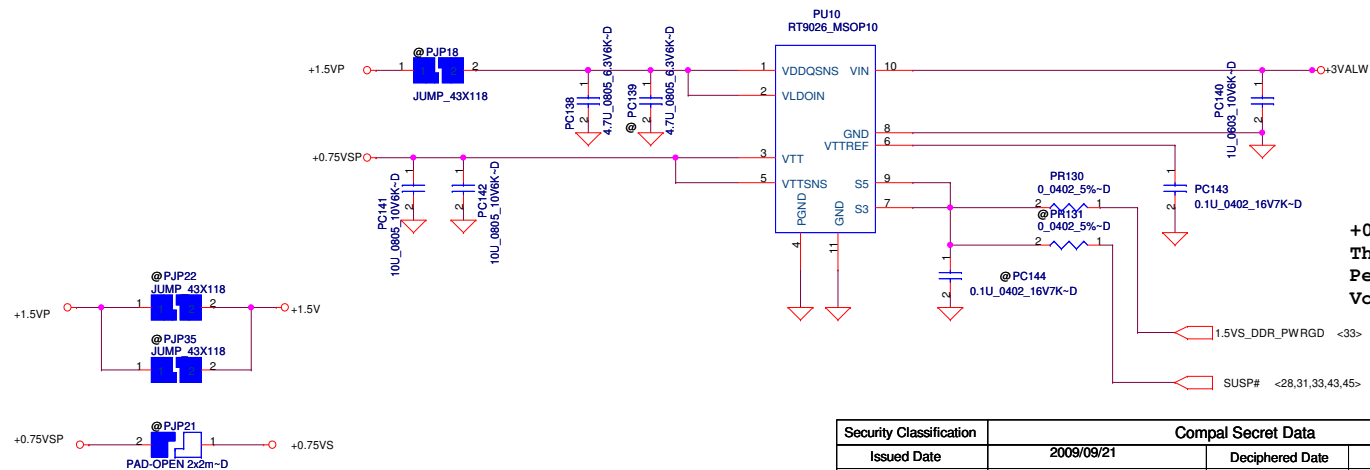
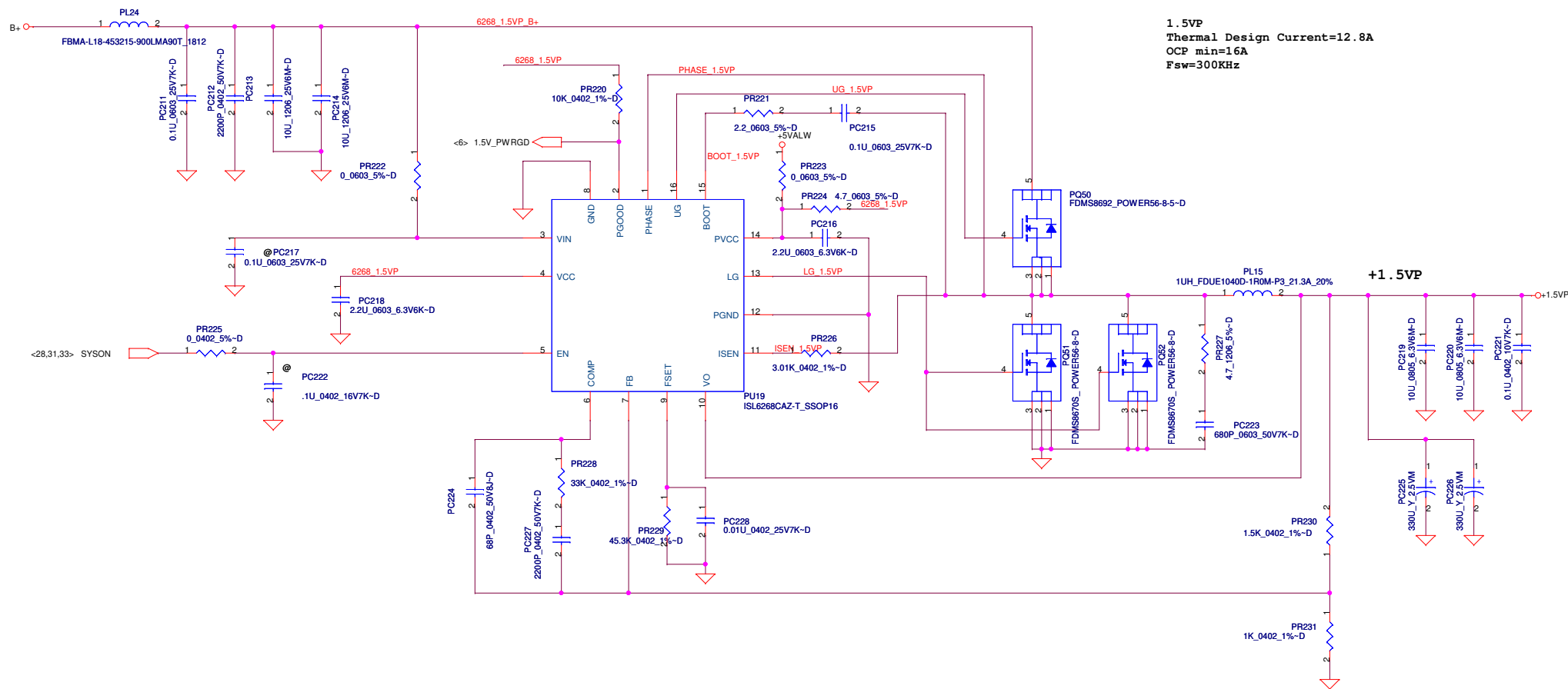


+1.05VSP
Thermal Desig Current=5A
OCP_min=9A
Fsw=300KHz

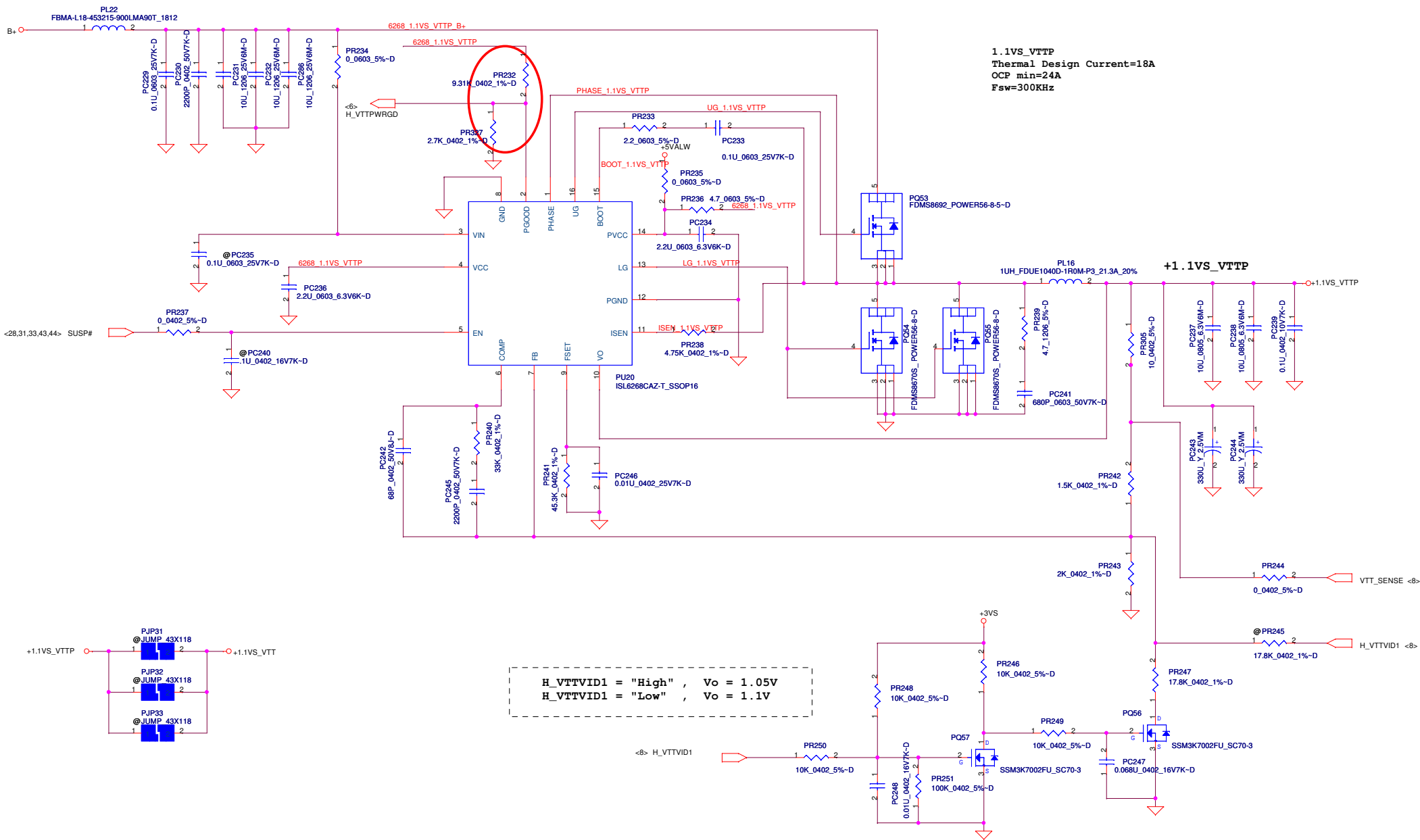


+1.8VSP
Thermal Desig Current=0.69A

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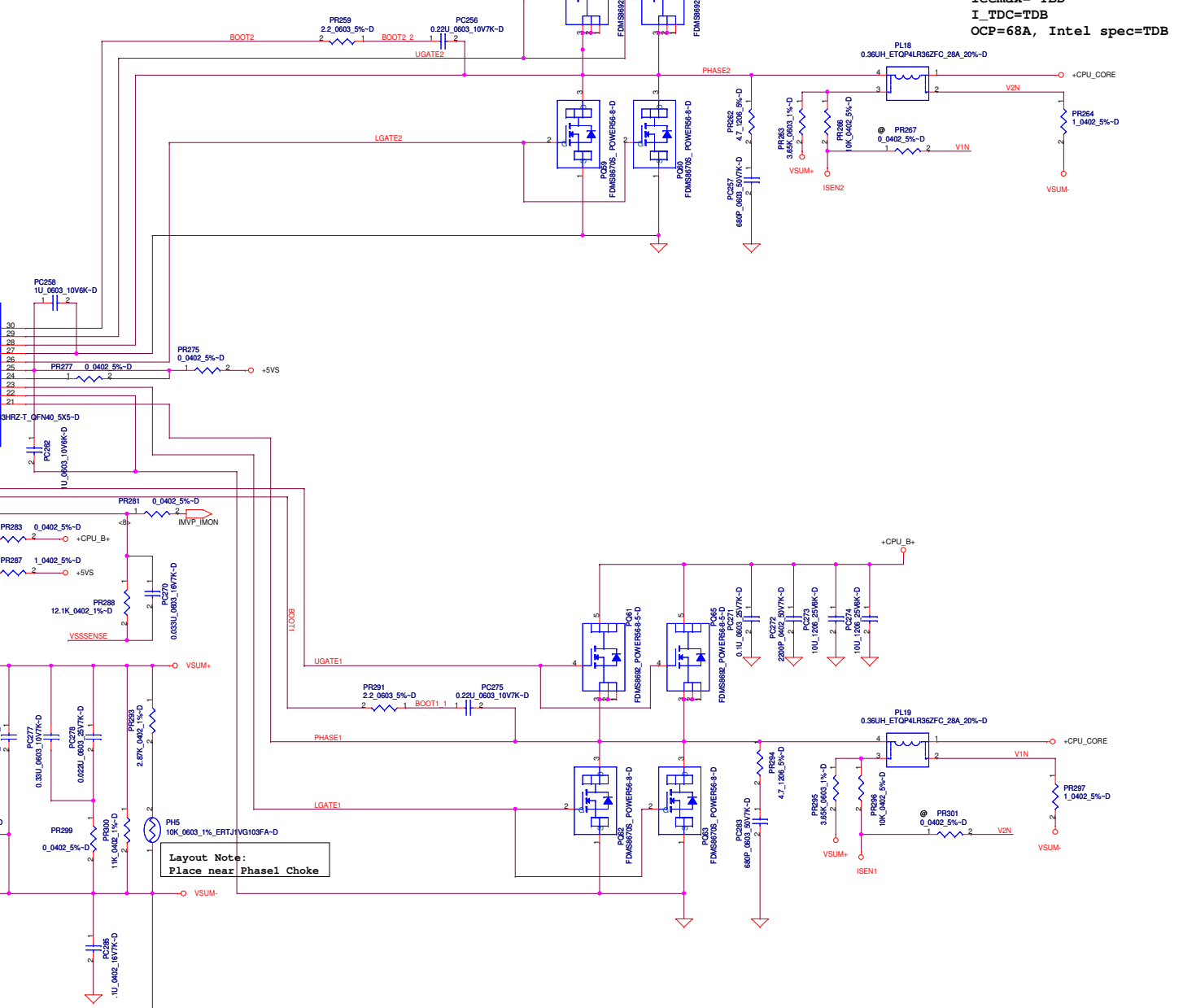
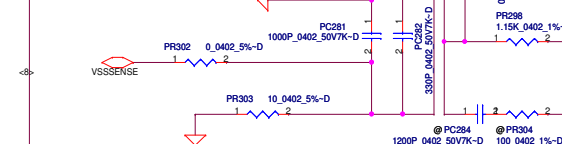
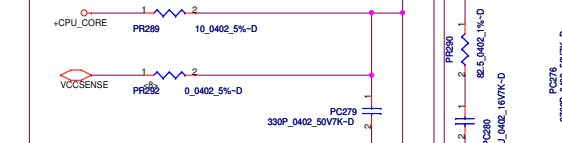
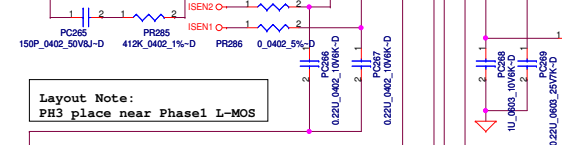
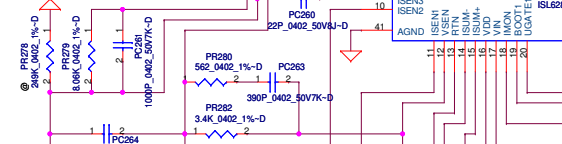
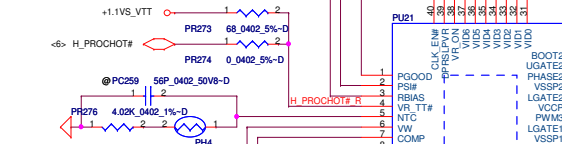
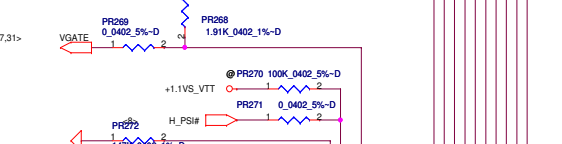
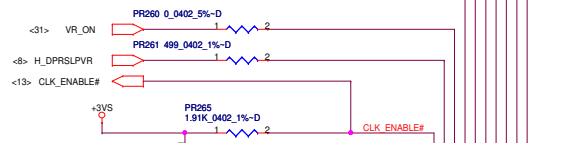
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								+1.1VS_VTTP			
								Size			
								Custom			
								Document Number			
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OCP calculation: Assume DCR=0.88mOhm
 $G1 = R_n / (R_n + R_{sum} / 3)$,
where $R_n = PR224 / (PR171 + PH5)$; $R_{sum} = PR143, PR215$
 $DROOP = 2 * (DCR / 2) * G1 * R_{droop} / R_i = 1.896mOhm$
where $R_{droop} = PR161$; $R_i = PR212$
 $I_{ocp} = 42.7uA * R_{droop} / DROOP \sim 68A$.



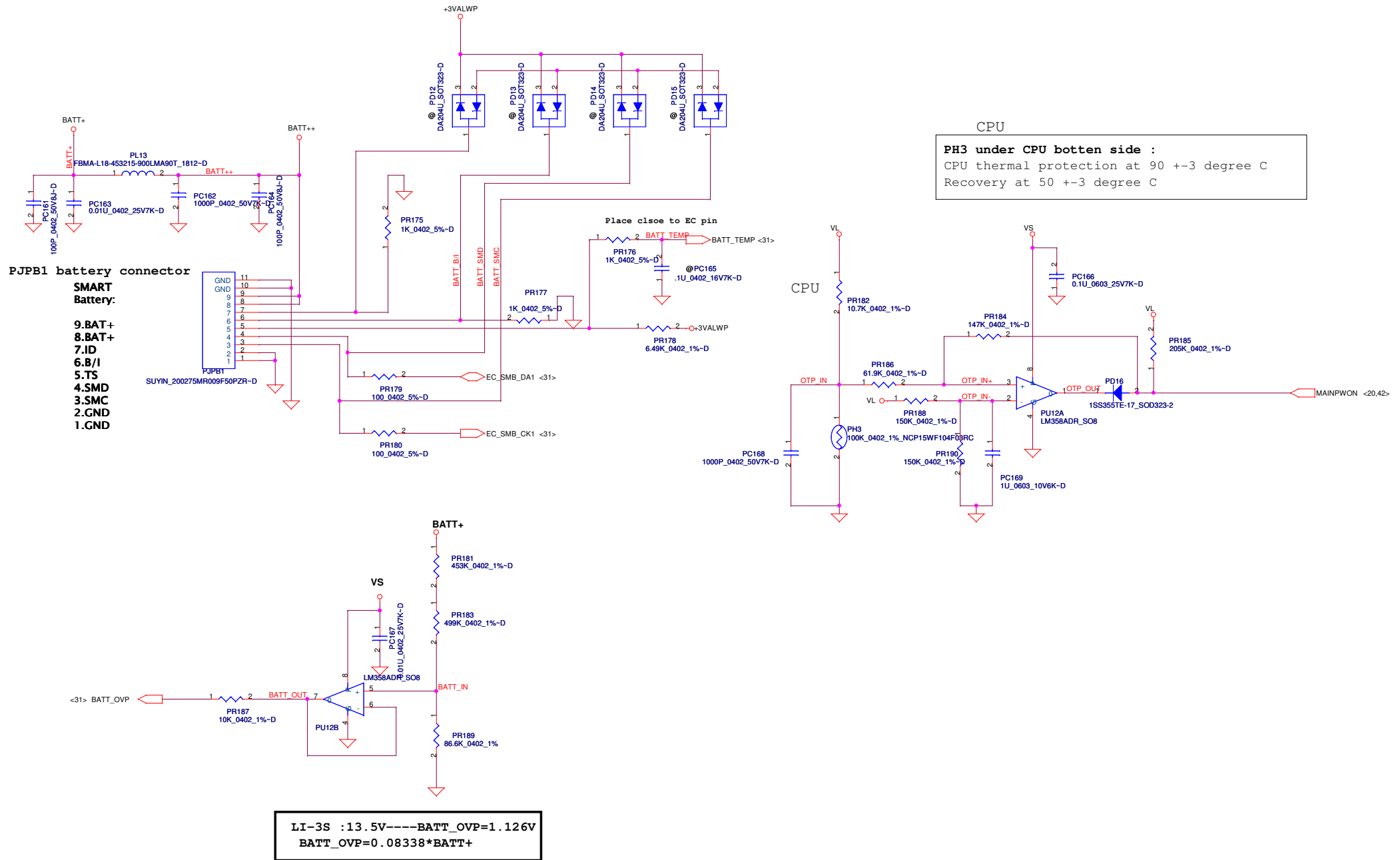
Iccmax= TBD
I_TDC=TDB
OCP=68A, Intel spec=TDB

Layout Note:
PH3 place near Phasel L-MOS

Layout Note:
Place near Phasel Choke

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Battery Connect/OTP



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								BATTERY CONN				
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	P51	+1.1VS_VTTP	08/31	Lin Will	Slove EMI	Add PL22 and Change PR233 form 0 ohm to 2.2 ohm.	X01
02	P53	+CPU_Core	08/31	Lin Will	Slove EMI	Change PR259 and PR291 from 0 ohm to 2.2 ohm.	X01
03	P55	+GFX_COREP	08/31	Lin Will	Adjust load-line and Imon	Change PR306 form 9.54K to 9.76K, PR210 from 22.3K to 24K and PC296 from 0.22uF to 0.033uF.	X01
04	P55	+GFX_COREP	08/31	Lin Will	Adjust output voltage ripple and thermal disipation	Add PQ46 and change PC289, PC290, PC301 from 4.7uF to 10uF, and PC105, PC106 from 330uF 9mohm to 330uF 6mohm.	X01
05	P43	+1.05VSP/+0.75VSP	10/14	Lin Will	Slove the IC input power sequence.	Change TPS51117 V5FILT and V5DRV from 5VS to 5VALW.	X02
06	P42	+3VALWP/+5VALWP	10/14	Lin Will	Slove EMI.	Change PJP19 to PL23, and PR59, PR60 from 0 ohm to 2.2 ohm.	X02
07	P44	+1.5VSP/+0.75VSP	10/14	Lin Will	Slove EMI.	Change PJP29 to PL24.	X02
08	P45	+1.1VS_VTTP	11/20	Lin Will	Low down the power consumption.	Change PR232 from 43.2K to 9.31K, and add PR327 2.7K.	X03
09	P41/P42	Charger +3VALWP/+5VALWP	11/20	Lin Will	1206 size shortage issue.	Change SE142475K8L(1206) to SE000006R8L(0805), and SE041224K8L(1206) to SE000005Z8L(0603).	X03
10	P42	+3VALWP/+5VALWP	11/20	Lin Will	When adapter inserts and pulls out quickly two twice, it will make TPS51427 out of electricity.	Add PR91,PR92,PR93 100K, PQ24 TP0610K, PQ10 DTC115EUA, and PD17 1SS355TE-17. But all unpop. Change PU5 to ISL6237, and add PJP24.	X03

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